Nakia 14'' N7 Schematics

Tiger Lake UP3 (15W)

2020-08

REV : A00

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Cover Page	
Size: A3	Document Number: NAKIA_SHURI_N7_TGL-U	Rev: A00
Date: Wednesday, August 05, 2020	Sheet 1 of 106	

Project code : 4PD0KW010001
MB PCB P/N : 19765
MB Revision : SD
DB PCB P/N : 19A90
DB Revision : SD

eDP 13" / 14.5" Panel
FHD / QHD
55
eDPx4
LCD1
DDI-A 4-lane

HDMI2.0
57
DDI 4-lane
Parade
PS8409A 57
DDI 4-lane

Flash ROM
XTL
X7101
SPI
CLK

TBT RETIMER
INTEL
Burnside BRIDGE
71
TCP0
TX+/-, RX+/- x 2
I2C

Type-C Port1
Option1: TBT / USB3.1/ DP/PD
Option2: / USB3.1/ DP/PD
73
CC control pin
TYPEC PD controller
TI SN1905024RJKR
72
SML1
USB2.0 D+/-

USB-A port1
35
USB3.0/2.0

USB BD
USB-A port2
35
USB3.0
USB 3.1
re-Driver
35
USB3.0
USB2.0
AUD Jack
microSD Card
SD3.0
33
Card Reader
Realtek
RTS5144
33
USB2.0

(2W, 4ohm)
2CH Speaker
Audio Codec
RealTek ALC3204
27
HDA
I2C

Camera module
on Panel side
Internal Digital MIC
Camera
55
I2C
USB2.0

Intel CPU
Tiger LAKE-U 4+2
1449 Pin
PCH-LP
4 TCSS Lanes
12 PCIe*3.0 Lanes (SATA*2, USB31*2)
1 PCIE4.0x4 Lanes
10 USB2.0
CNVi2.0
ESPI / SPI
HDA/SNDW
CSI
(Remove SD/EMMC)
X1801
X1802
3,4,5,6,7,8,9,10,11,15
16,17,18,19,20,21,22,23

LPDDR4x Channel A
MD x32
Type-3: 4267 8/16GB
12
NON-INTERLEAVE MODE
LPDDR4x Channel B
MD x32
Type-3: 4267 8/16GB
13

PCIEx4
M.2 2242-B key Myraid
M.2 2280 M-key Aaeon2
Co-lay
SATAx1
NVMe SSD
SATA SSD
90

CNVi/PCIE x 1
M.2 WLAN
on Board SIP module
62

SPI
Flash ROM 32MB
MX25L25673GM2I
25

SPI
TPM
NPCT750JABYX
91

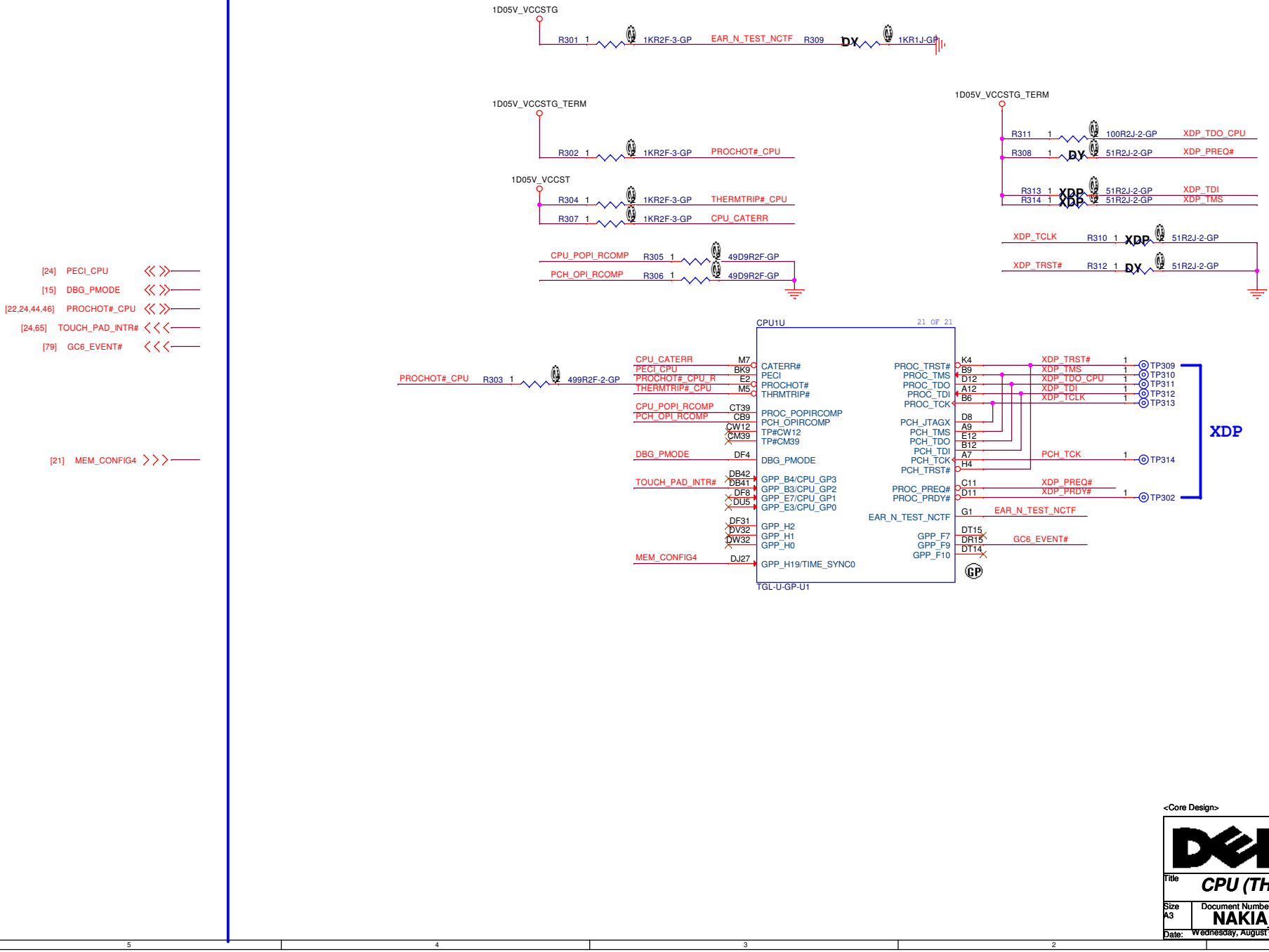
eSPI debug port
68
eSPI
EC
MEC1515 X2401
24
KB/TP Conn
65
Thermal & Fan
26

ISH I2C
3 Axis Accelerometer
ST LIS2DH12
70

LANE 5~8
PCIE4 x 4
GPU X7901
NVIDIA
N17S-G3/G5 18W
76-80
GDDR5
VRAM(GDDR5) *2
2GB
81-82

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: Block Diagram
Size: A3
Document Number: NAKIA_SHURI_N7_TGL-U
Rev: A00
Date: Wednesday, August 05, 2020
Sheet 2 of 106

SSID = CPU



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*CPU (THML/JTAG)*	
Size A3	Document Number NAKIA_SHURI_N7_TGL-U	Rev A00
Date: Wednesday, August 05, 2020	Sheet 3 of 106	

SSID = CPU

eDP

[55] eDP_TX_CPU_N0
[55] eDP_TX_CPU_P0
[55] eDP_TX_CPU_N1
[55] eDP_TX_CPU_P1
[55] eDP_TX_CPU_N2
[55] eDP_TX_CPU_P2
[55] eDP_TX_CPU_N3
[55] eDP_TX_CPU_P3
[55] eDP_AUX_CPU_N
[55] eDP_AUX_CPU_P
[55] EDP_HPD
[24] L_BKLT_EN
[55] eDP_VDD_EN
[55] L_BKLT_CTRL

HDMI

[57] HDMI_DDI_TX_P3
[57] HDMI_DDI_TX_N3
[57] HDMI_DDI_TX_P0
[57] HDMI_DDI_TX_N0
[57] HDMI_DDI_TX_P1
[57] HDMI_DDI_TX_N1
[57] HDMI_DDI_TX_P2
[57] HDMI_DDI_TX_N2

[57] CPU_DPB_CTRL_CLK
[57] CPU_DPB_CTRL_DATA

[57] CPU_DISP_HPDB

TBT

[71] USB1_TCSS_TX_N0
[71] USB1_TCSS_TX_P0
[71] USB1_TCSS_TX_N1
[71] USB1_TCSS_TX_P1
[71] USB1_TCSS_RX_N0
[71] USB1_TCSS_RX_P0
[71] USB1_TCSS_RX_N1
[71] USB1_TCSS_RX_P1
[71] USB1_TCSS_AUX_N
[71] USB1_TCSS_AUX_P
[71] TBT_LSX0_TXD
[15,71] TBT_LSX0_RXD

Other

[15] GPP_E21
[15] GPP_D12
[15] GPP_D10
[65] KB_DET#

Type-A (IO)

[66] USB_OC1#

CPU1A — 1 OF 21

eDP_TX_CPU_P3 AC2 — DDIA_TXP3
eDP_TX_CPU_N3 AC1 — DDIA_TXN3
eDP_TX_CPU_P2 AD2 — DDIA_TXP2
eDP_TX_CPU_N2 AD1 — DDIA_TXN2
eDP_TX_CPU_P1 AF1 — DDIA_TXP1
eDP_TX_CPU_N1 AF2 — DDIA_TXN1
eDP_TX_CPU_P0 AG2 — DDIA_TXP0
eDP_TX_CPU_N0 AG1 — DDIA_TXN0
eDP_AUX_CPU_P AJ2 — DDIA_AUX_P
eDP_AUX_CPU_N AJ1 — DDIA_AUX_N

DN4 — GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD
DT6 — GPP_E23/DDPA_CTRLDATA

EDP_HPD DR5 — GPP_E14/DDSP_HPDA/DISP_MISCA

HDMI_DDI_TX_P3 T12 — DDIB_TXP3
HDMI_DDI_TX_N3 T11 — DDIB_TXN3
HDMI_DDI_TX_P0 Y11 — DDIB_TXP2
HDMI_DDI_TX_N0 Y9 — DDIB_TXN2
HDMI_DDI_TX_P1 T9 — DDIB_TXP1
HDMI_DDI_TX_N1 P9 — DDIB_TXN1
HDMI_DDI_TX_P2 V11 — DDIB_TXP0
HDMI_DDI_TX_N2 V9 — DDIB_TXN0
AB9 — DDIB_AUX_P
AD9 — DDIB_AUX_N

3D3V_S0

CPU_DPB_CTRL_CLK DM29 — GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN
CPU_DPB_CTRL_DATA DK27 — GPP_H17/DDPB_CTRLDATA

CPU_DISP_HPDB DG43 — GPP_A18/DDSP_HPDB/DISP_MISCB/I2S4_RXD

R406 10KR2J-3-GP 2 1
KB_DET# DG47 — GPP_A21/DDPC_CTRLCLK/I2S5_TXD
DJ47 — GPP_A22/DDPC_CTRLDATA/I2S5_RXD

TBT_LSX0_TXD DU8 — GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD
TBT_LSX0_RXD DV8 — GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD

GPP_E21 DF6 — GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD
DD6 — GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD

GPP_D10 DN23 — GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#
DM23 — GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK

GPP_D12 DK23 — GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO
DN21 — GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI

R404 (DY) 1 100KR2J-1-GP CPU_DISP_HPD1 — DF43 GPP_A17/DISP_MISCC/I2S4_TXD
DF45 — GPP_A19/DDSP_HPD1/DISP_MISC1/I2S5_SCLK
DF47 — GPP_A20/DDSP_HPD2/DISP_MISC2/I2S5_SFRM

3D3V_S5_VCCPRIM
R403 2 1 10KR2J-3-GP USB_OC1# — DH52
R405 2 1 10KR2J-3-GP USB_OC2# — DK45 GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1
3D3V_S5_VCCPRIM
GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK

eDP_VDD_EN DM8 — EDP_VDDEN
L_BKLT_EN DN8 — EDP_BKLTEN
L_BKLT_CTRL DG10 — EDP_BKLTCTL

TGL-U-GP-U1

TCP0_TXRX_P1 AY2 — USB1_TCSS_RX_P1
TCP0_TXRX_N1 AY1 — USB1_TCSS_RX_N1
TCP0_TXRX_P0 BB1 — USB1_TCSS_RX_P0
TCP0_TXRX_N0 BB2 — USB1_TCSS_RX_N0
TCP0_TX_P1 AM5 — USB1_TCSS_TX_P1
TCP0_TX_N1 AM7 — USB1_TCSS_TX_N1
TCP0_TX_P0 AT7 — USB1_TCSS_TX_P0
TCP0_TX_N0 AT5 — USB1_TCSS_TX_N0
TCP0_AUX_P AP7 — USB1_TCSS_AUX_P
TCP0_AUX_N AP5 — USB1_TCSS_AUX_N

TBT

TCP1_TXRX_P1 AT2
TCP1_TXRX_N1 AT1
TCP1_TXRX_P0 AU1
TCP1_TXRX_N0 AU2
TCP1_TX_P1 AD5
TCP1_TX_N1 AD7
TCP1_TX_P0 AH7
TCP1_TX_N0 AH5
TCP1_AUX_P AF7
TCP1_AUX_N AF5

TCP2_TXRX_P1 BF1
TCP2_TXRX_N1 BF2
TCP2_TXRX_P0 BE2
TCP2_TXRX_N0 BE1
TCP2_TX_P1 BD7
TCP2_TX_N1 BD5
TCP2_TX_P0 AY5
TCP2_TX_N0 AY7
TCP2_AUX_P BB5
TCP2_AUX_N BB7

TCP3_TXRX_P1 BK1
TCP3_TXRX_N1 BK2
TCP3_TXRX_P0 BJ2
TCP3_TXRX_N0 BJ1
TCP3_TX_P1 BM7
TCP3_TX_N1 BM5
TCP3_TX_P0 BH5
TCP3_TX_N0 BH7
TCP3_AUX_P BK5
TCP3_AUX_N BK7

TC_RCOMP_P AN2 — TCSS_RCOMP_P
TC_RCOMP_N AN1 — TCSS_RCOMP_N
R402 1 — 150R2F-1-GP

DSI_DE_TE_2 M8

DDI_RCOMP AB1 — DISP_RCOMP
R401 1 — 150R2F-1-GP

DISP_UTILS/DSI_DE_TE_1 CE4

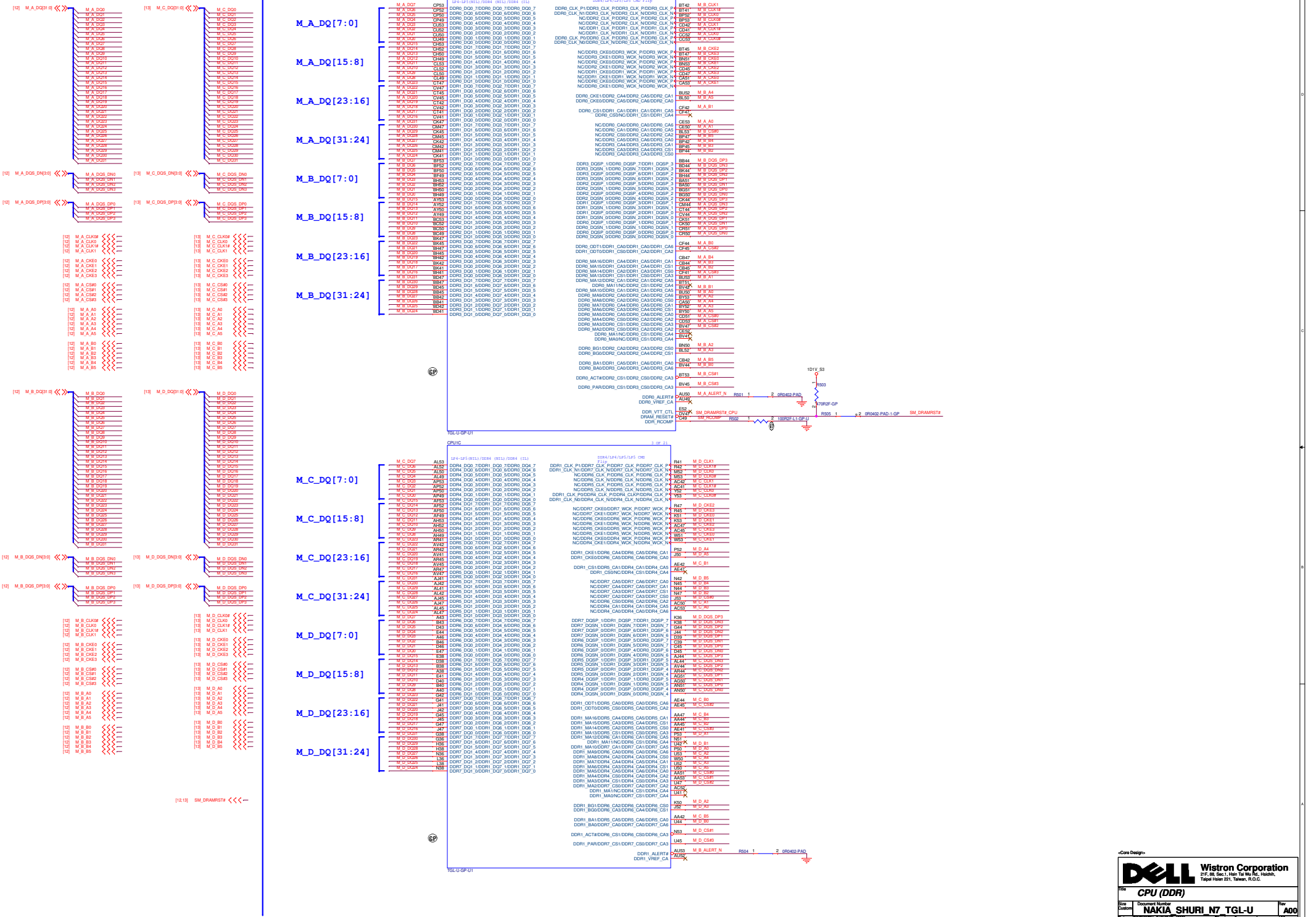
GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDI/EDP/TBT/TPC/)
Size: A3
Document Number: NAKIA_SHURI_N7_TGL-U
Rev: A00
Date: Wednesday, August 05, 2020
Sheet 4 of 106

SSID = CPU

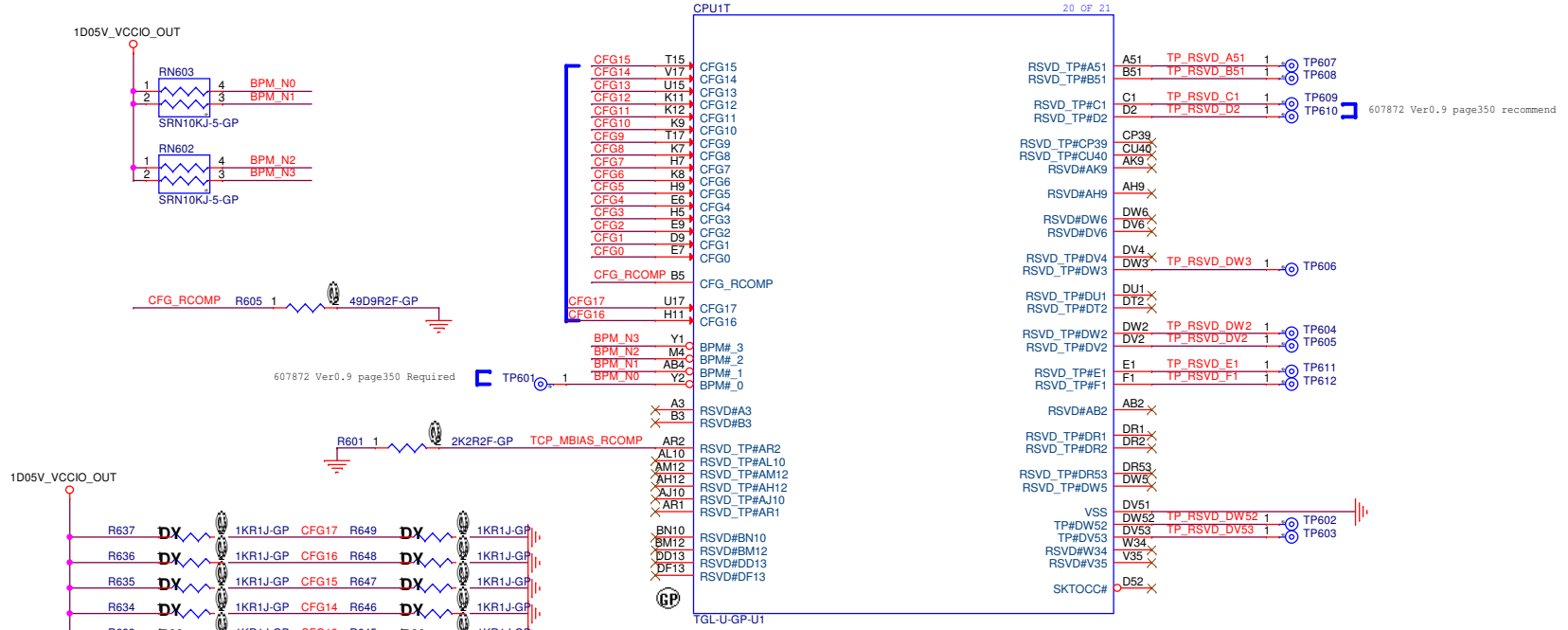


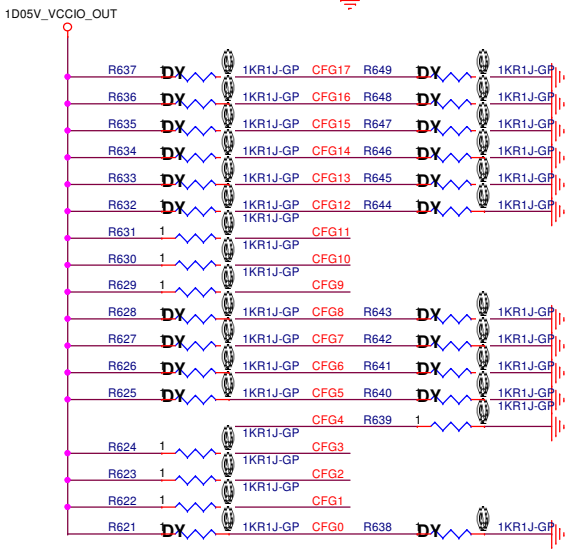
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR)

Size	Document Number	Rev
Custom	NAKIA_SHURI_N7_TGL-U	A00
Date: Wednesday, August 05, 2020	Sheet 5 of 108	

SSID = CPU





CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CFG/IST)

Size: A3 | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 6 of 106

SSID = CPU

[46] VCCCORE_SENSE
[46] VSSCORE_SENSE
[46] SVID_ALERT#_CPU
[46] SVID_CLK_CPU
[46] SVID_DATA_CPU

CPU1M 13 OF 21

VCCIN	A24	VCCIN	G32
VCCIN	A26	VCCIN	H24
VCCIN	A29	VCCIN	H26
VCCIN	A30	VCCIN	H30
VCCIN	A33	VCCIN	H32
VCCIN	A35	VCCIN	J1
VCCIN	AY39	VCCIN	J2
VCCIN	B24	VCCIN	K1
VCCIN	B26	VCCIN	K2
VCCIN	B29	VCCIN	K24
VCCIN	B30	VCCIN	K26
VCCIN	B33	VCCIN	K30
VCCIN	B35	VCCIN	K32
VCCIN	BA10	VCCIN	L24
VCCIN	BA40	VCCIN	L26
VCCIN	BB39	VCCIN	L30
VCCIN	BB9	VCCIN	L32
VCCIN	BC10	VCCIN	N24
VCCIN	BC40	VCCIN	N26
VCCIN	BD39	VCCIN	N30
VCCIN	BD9	VCCIN	N32
VCCIN	BE10	VCCIN	P24
VCCIN	BE40	VCCIN	P26
VCCIN	BF9	VCCIN	P28
VCCIN	BG10	VCCIN	P30
VCCIN	BG40	VCCIN	P32
VCCIN	BH12	VCCIN	T21
VCCIN	BH39	VCCIN	T23
VCCIN	BH9	VCCIN	T25
VCCIN	BJ10	VCCIN	T27
VCCIN	BJ40	VCCIN	T31
VCCIN	BK39	VCCIN	U23
VCCIN	BL10	VCCIN	U27
VCCIN	BL40	VCCIN	U29
VCCIN	BM39	VCCIN	U31
VCCIN	BN40	VCCIN	U33
VCCIN	BP12	VCCIN	V23
VCCIN	BP39	VCCIN	V25
VCCIN	BR10	VCCIN	V27
VCCIN	BR40	VCCIN	V29
VCCIN	BT12	VCCIN	V31
VCCIN	BT39	VCCIN	V33
VCCIN	BU10	VCCIN	W22
VCCIN	BU40	VCCIN	W24
VCCIN	BV12	VCCIN	W28
VCCIN	BY12	VCCIN	W32
VCCIN	CA10	VCCIN	
VCCIN	CB12	R38	VCCCORE_SENSE
VCCIN	D24	VCCIN_SENSE	
VCCIN	D26	R37	VSSCORE_SENSE
VCCIN	D29	VSSIN_SENSE	
VCCIN	D30	M12	SVID_DATA_CPU
VCCIN	D33	VIDSOUT	
VCCIN	D35	M11	SVID_CLK_CPU
VCCIN	E24	VIDSCK	
VCCIN	E26	P12	SVID_ALERT#_CPU_R
VCCIN	E27	VIDALERT#	
VCCIN	E29		
VCCIN	E30		
VCCIN	E32		
VCCIN	E33		
VCCIN	G2		
VCCIN	G24		
VCCIN	G26		
VCCIN	G30		

TGL-U-GP-U1

1D05V_VCCST

R703 1 — 2 100R2F-L1-GP-U SVID_DATA_CPU
R701 2 — 1 56R2J-4-GP SVID_ALERT#_CPU
R707 DY 1 56R2J-4-GP SVID_CLK_CPU

3.Length matchin 25mil, and close SOC in 2inch "

Layout note: **Layout Note:**

1. Place close to CPU within 2"
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

VCCIN

R704 1 — 2 100R2F-L1-GP-U VCCCORE_SENSE
R705 1 — 2 100R2F-L1-GP-U VSSCORE_SENSE

R706 0R0402-PAD 1 2 SVID_ALERT#_CPU

<Core Design>

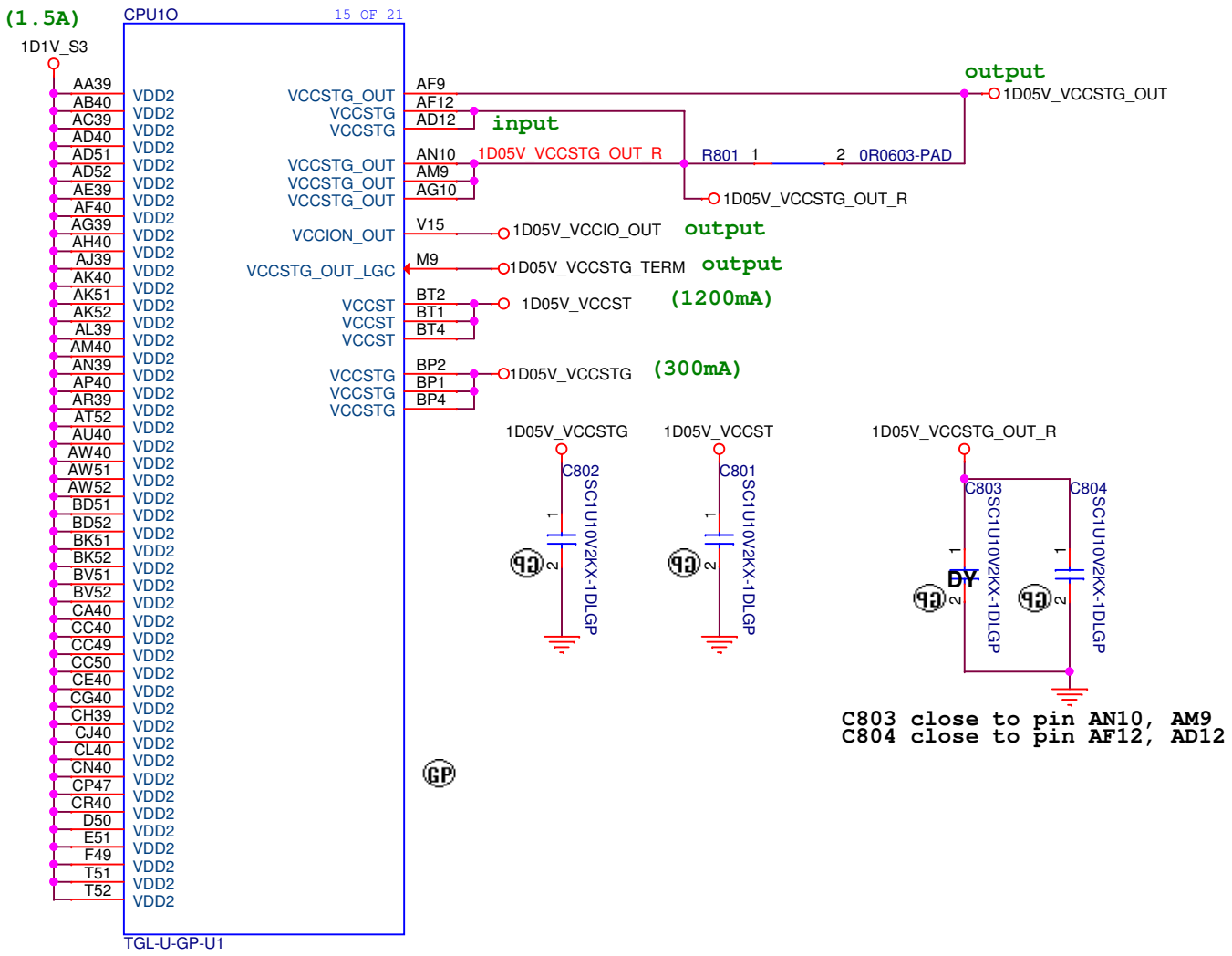
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VCCIN/VID)***

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 7 of 106

SSID = CPU



Lack of VCCPLL_OC / VCC1P8A / VCCPLL

<Core Design>

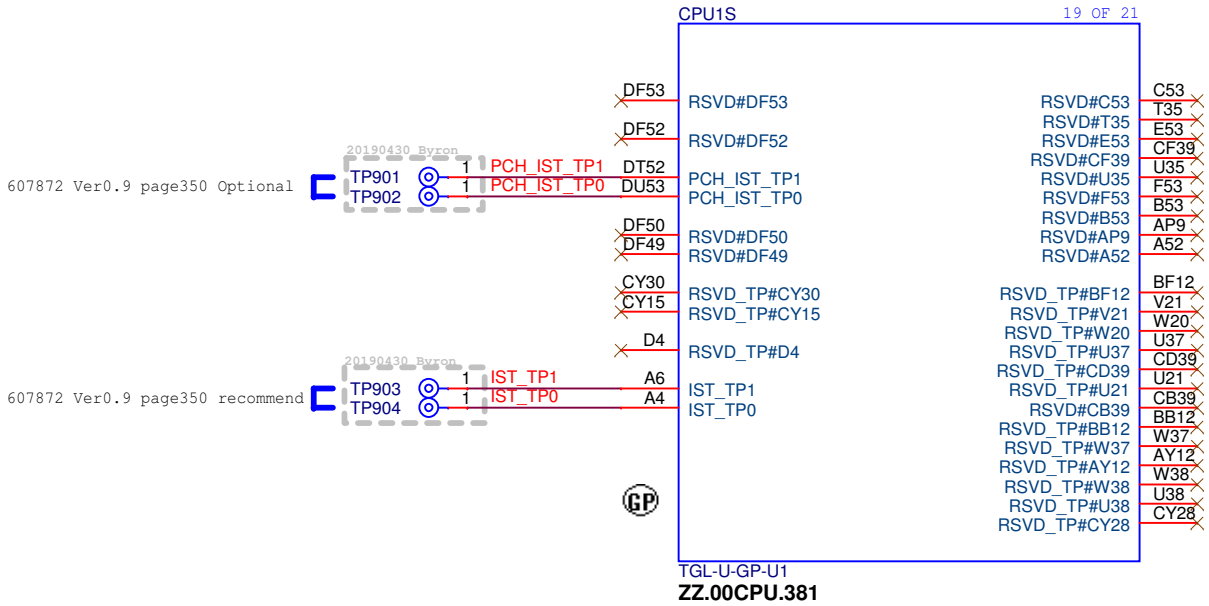
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

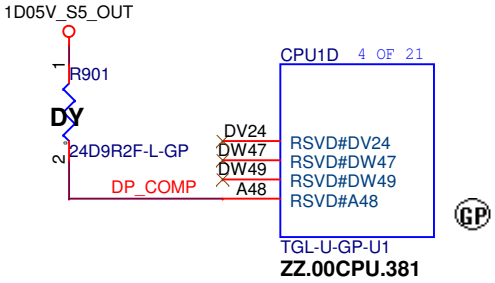
Title: *CPU (VDDQ/VCC/VCCST)*

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 8 of 106

SSID = CPU





<Core Design>

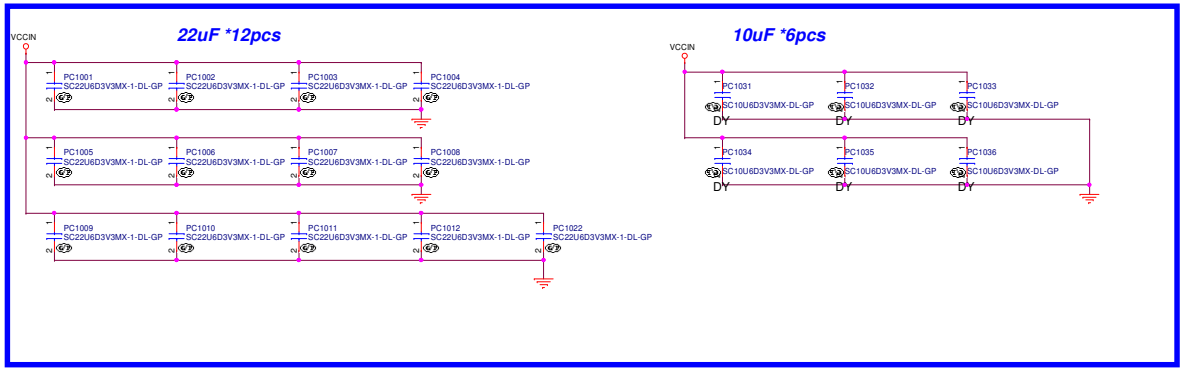
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

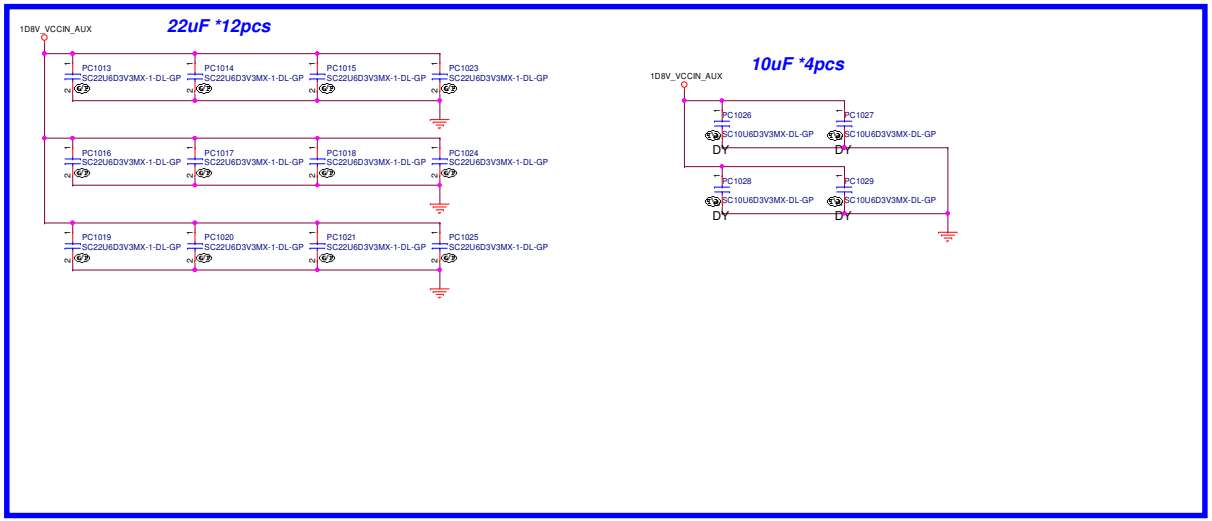
Title: *CPU (RSVD)*

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 9 of 106

SSID = CPU





<Core Design>

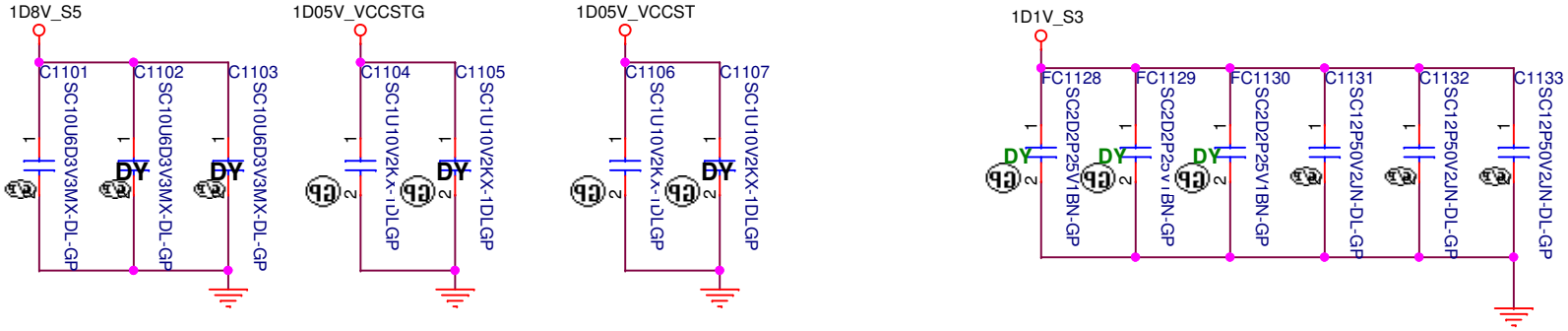
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CORE Power Cap1)

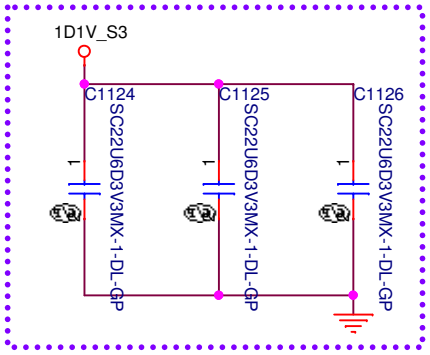
Size	Document Number	Rev
A2	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 10 of 106

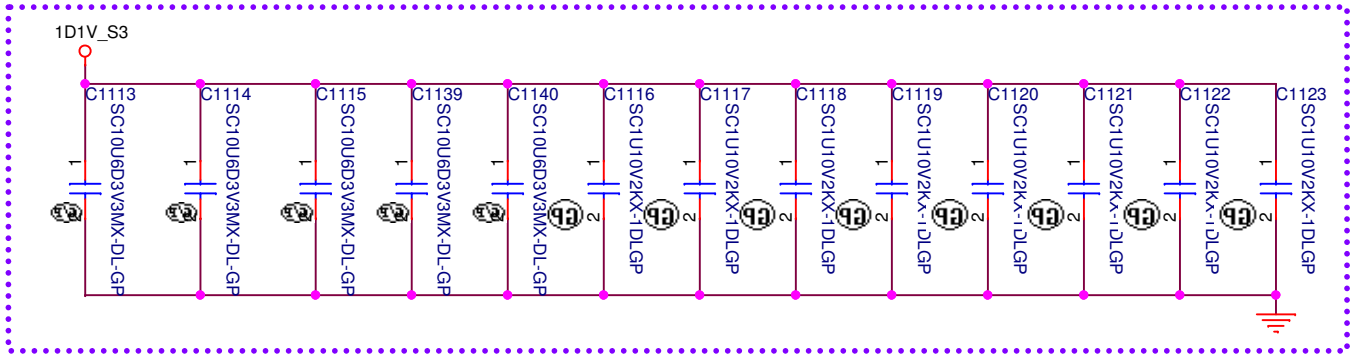
SSID = CPU



PLACE on CPU Same Side



PLACE on BACK SIDE



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

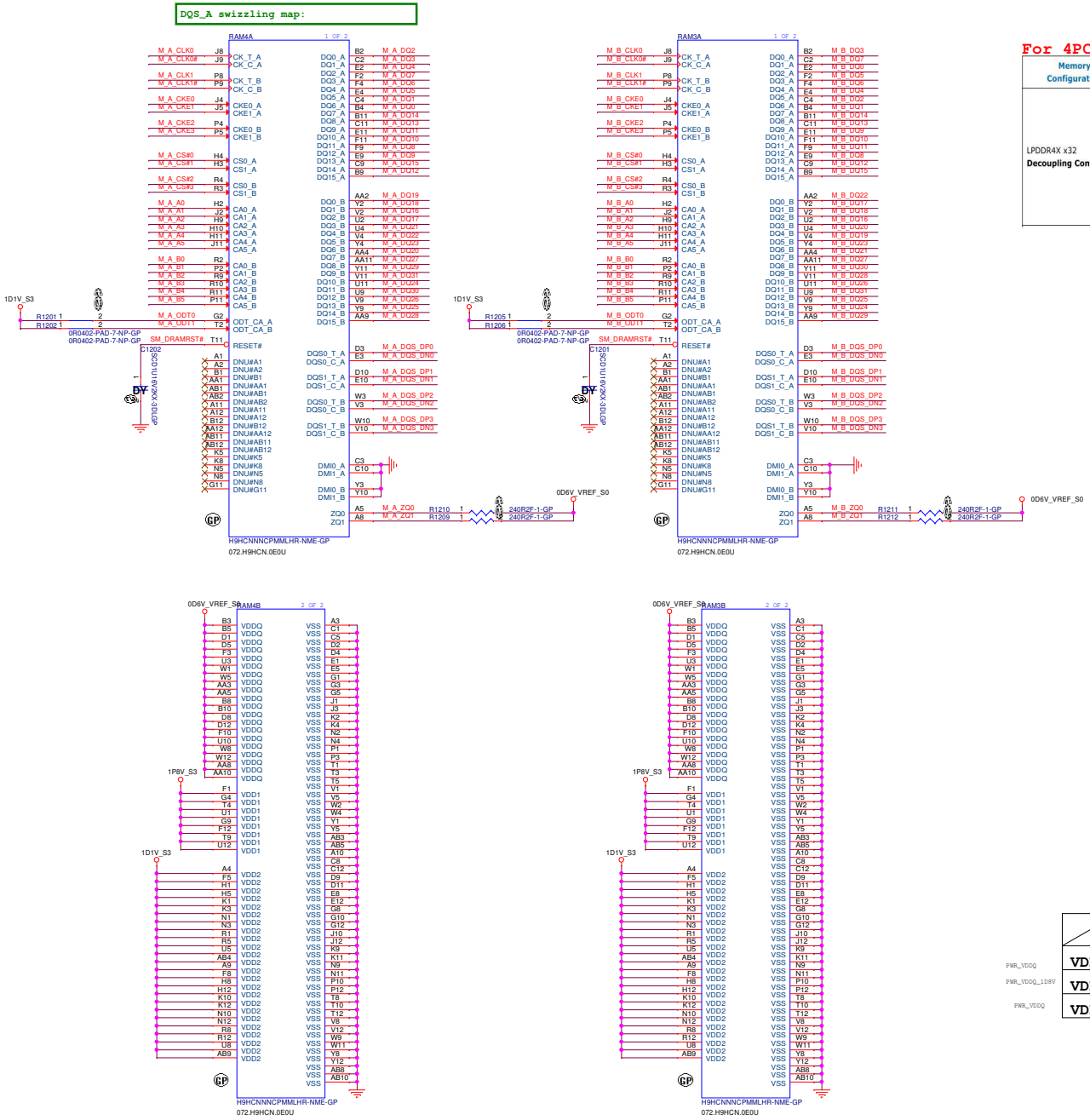
Title: *CPU (Power Cap2)*

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 11 of 106

SSID = MEMORY

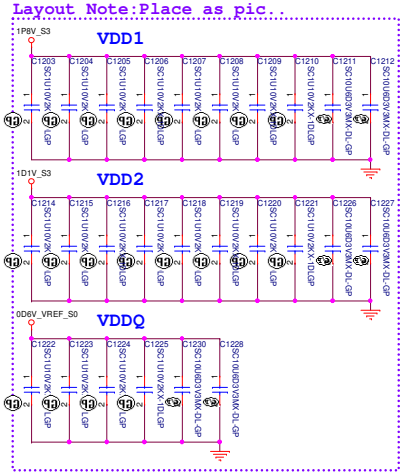
DQS_A swizzling map:



For 4PCS RAM place

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
LPDDR4X x32 **Decoupling Config-1**	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDDQ	4 per Dram, 2 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute	5x 10µF (0603)

Layout Note:Place as pic.



	LPDDR4		LPDDR4X		
VDDQ	1.1V	410mA	0.6V	185mA	PWR_VDDQ_VTT
VDD1	1.8V	6.8mA	1.8V	12mA	PWR_VDDQ_1D8V
VDD2	1.1V	290mA	1.1V	465mA	1D1V_S3

PWR_VDDQ
PWR_VDDQ_1D8V
PWR_VDDQ

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

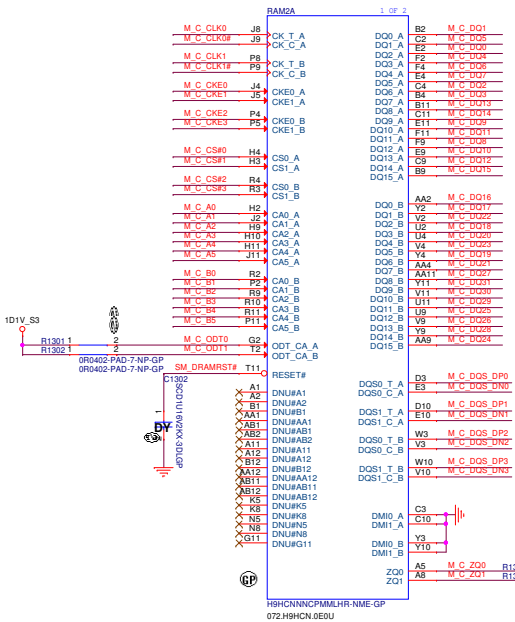
Title: DDR (DDR4-CHA)

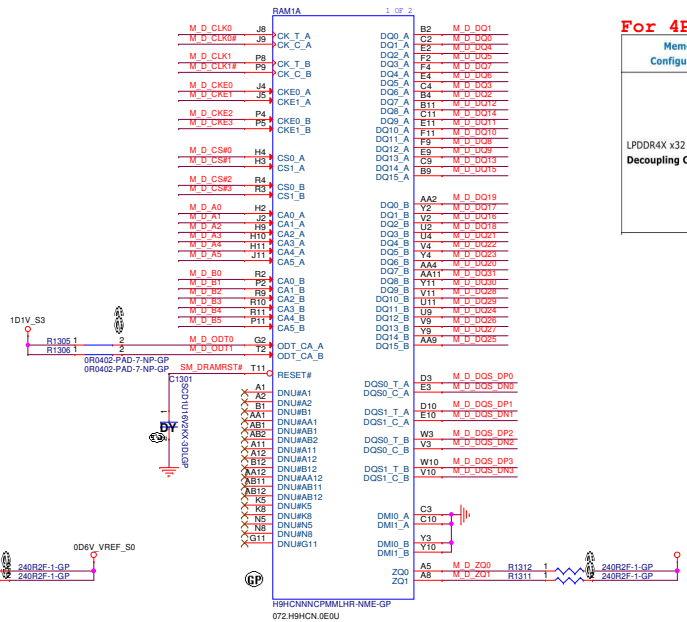
Size: A2 | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00

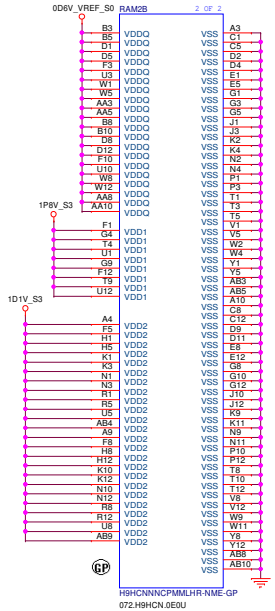
Date: Wednesday, August 05, 2020 | Sheet 12 of 106

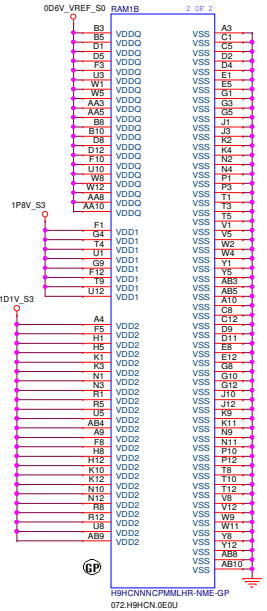
SSID = MEMORY

DQS_B swizzling map:





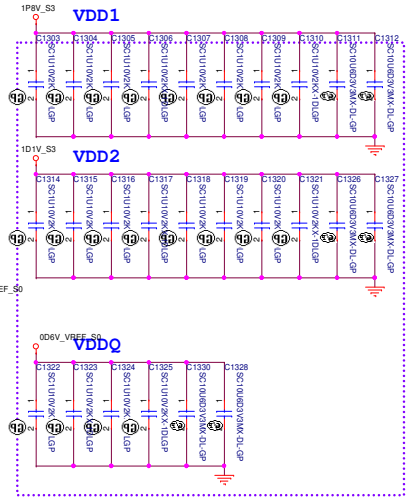




For 4PCS RAM place

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
LPDDR4X x32 **Decoupling Config-1**	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDDQ	4 per Dram, 2 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute among all Drams	5x 10µF (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1µF (0402)
		evenly distribute	5x 10µF (0603)

Layout Note:Place as pic..



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHB)

Size: A2 | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 13 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
DDR (RSVD) (DDR4-CHA1)

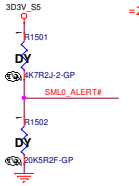
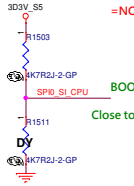
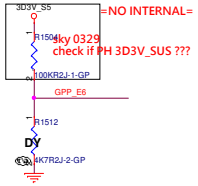
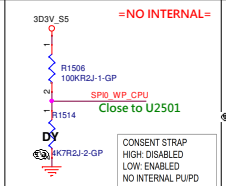
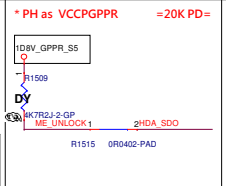
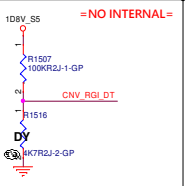
Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

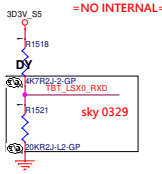
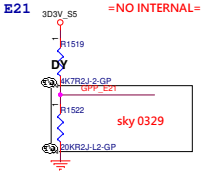
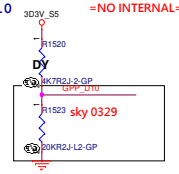
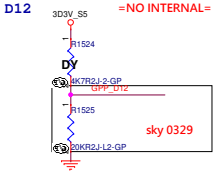
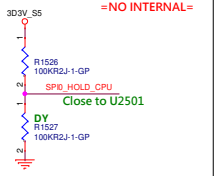
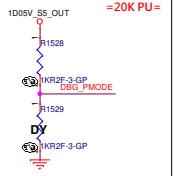
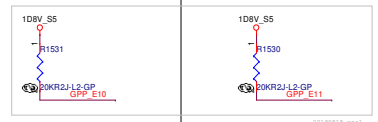
Date: Wednesday, August 05, 2020 Sheet 14 of 106

SSID = CPU

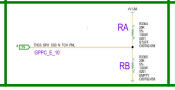
[18,24,25,91] SPI0_SI_CPU
[18,24,25] SPI0_WP_CPU
[18,24,25] SPI0_HOLD_CPU

[21,61] CNV_RGI_DT
[18] SML0_ALERT#
[18] GPP_E6
[19] HDA_SDO
[4,71] TBT_LSX0_RXD
[4] GPP_D10
[3] DBG_PMODE
[4] GPP_D12
[4] GPP_E21
[18] GPP_E10
[18] GPP_E11

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)
Schematic				=20K PD=			
High	ESPI Disable	Disable	Enable	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)	Disable	OVERRIDEN	INTEGRATED CNVI DISABLE
Low	Enable =default=	Enable	Disable	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Enable	SECURITY MEASURES NOT OVERRIDEN	INTEGRATED CNVI ENABLE

GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	A0		GPP_E10	GPP_E11
Schematic	E19 	E21 	D10 	D12 				
High	3.3V	3.3V	3.3V	3.3V	Disable	DFXTESTMODE DISABLED (DEFAULT)		
Low	1.8V	1.8V	1.8V	1.8V	Enable	DFXTESTMODE ENABLED		

Original Ref.

GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
ESPI OR EC LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PD 20K	BOOT HALT HIGH - DISABLED LOW- ENABLED NO INTERNAL PU/PD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PU/PD	CPUNSSC CLOCK FREQ HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL) LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PD 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVERRIDEN LOW: SECURITY MEASURES NOT OVERRIDEN WEAK INTERNAL PD 20K	M.2 CNVI MODES LOW-> INTEGRATED CNVI ENABLE HIGH-> INTEGRATED CNVI DISABLE NO INTERNAL PU/PD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD
TBT LSX #1	**TBT LSX #2**	**TBT LSX #3**	**A0**	**GPP_E10**	**GPP_E11**		
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD				

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size	Document Number	Rev
A2	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 15 of 106

SSID = PCH

GPU

[76] GFX_PCIE_TX_P0
[76] GFX_PCIE_TX_N0
[76] GFX_PCIE_RX_P0
[76] GFX_PCIE_RX_N0

[76] GFX_PCIE_TX_P1
[76] GFX_PCIE_TX_N1
[76] GFX_PCIE_RX_P1
[76] GFX_PCIE_RX_N1

[76] GFX_PCIE_TX_P2
[76] GFX_PCIE_TX_N2
[76] GFX_PCIE_RX_P2
[76] GFX_PCIE_RX_N2

[76] GFX_PCIE_TX_P3
[76] GFX_PCIE_TX_N3
[76] GFX_PCIE_RX_P3
[76] GFX_PCIE_RX_N3

M.2 SSD

[63] SSD_PCIE_TX_P1
[63] SSD_PCIE_TX_N1
[63] SSD_PCIE_RX_P1
[63] SSD_PCIE_RX_N1

[63] SSD_PCIE_TX_P2
[63] SSD_PCIE_TX_N2
[63] SSD_PCIE_RX_P2
[63] SSD_PCIE_RX_N2

[63] SSD_PCIE_TX_P3
[63] SSD_PCIE_TX_N3
[63] SSD_PCIE_RX_P3
[63] SSD_PCIE_RX_N3

[63] SSD_SATA_TX_P
[63] SSD_SATA_TX_N
[63] SSD_SATA_RX_P
[63] SSD_SATA_RX_N

[63] M2_PEDET1
[63] M2_DEVSLP1

WLAN

[61] WLAN_PCIE_TX_P
[61] WLAN_PCIE_TX_N
[61] WLAN_PCIE_RX_P
[61] WLAN_PCIE_RX_N
[61] WLAN_RF_DIS#

USB1

USB3.2 Type-A Port1 (MB)

[35] USB1_USB31_TX_P
[35] USB1_USB31_TX_N
[35] USB1_USB31_RX_P
[35] USB1_USB31_RX_N

[35] USB1_USB20_P
[35] USB1_USB20_N

[35] USB_OC0#

USB2

USB3.2 Type-A Port2 (IO)

[66] USB2_USB31_TX_P
[66] USB2_USB31_TX_N
[66] USB2_USB31_RX_P
[66] USB2_USB31_RX_N

[66] USB2_USB20_P
[66] USB2_USB20_N

Card Reader

[66] CARD1_USB20_P
[66] CARD1_USB20_N

Camera

[55] CCD_USB20_P
[55] CCD_USB20_N

Finger Print

[92] FP1_USB20_N
[92] FP1_USB20_P

TBT

[72] USB3_USB20_P
[72] USB3_USB20_N

BT

[61] BT_USB20_P
[61] BT_USB20_N

PD

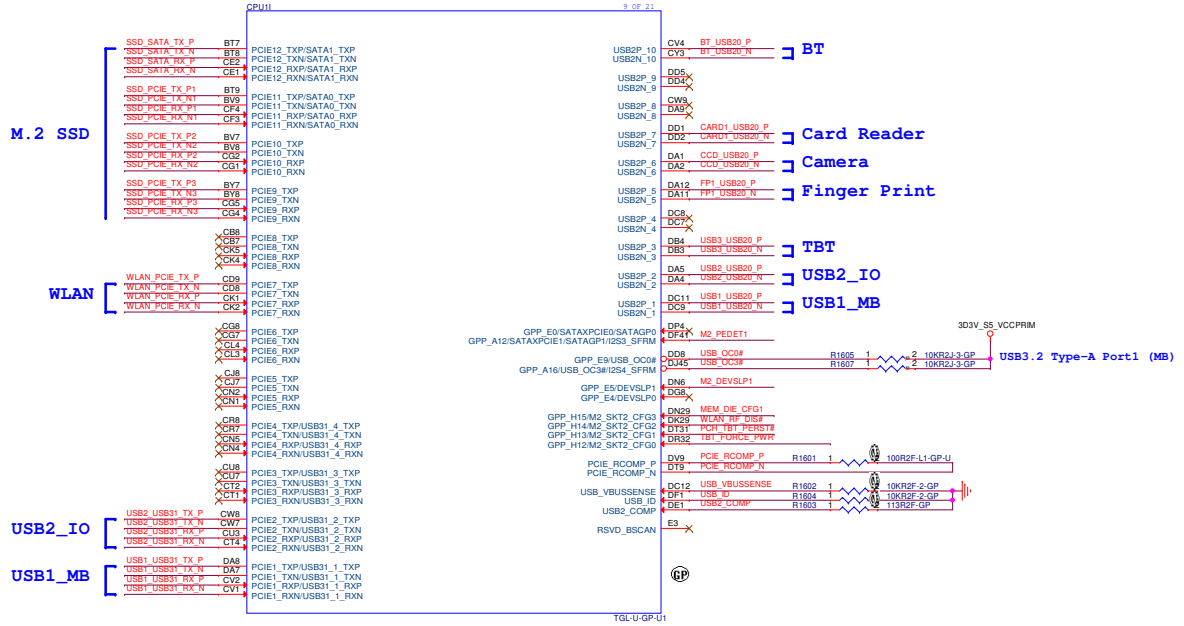
[72] USB_OC3#

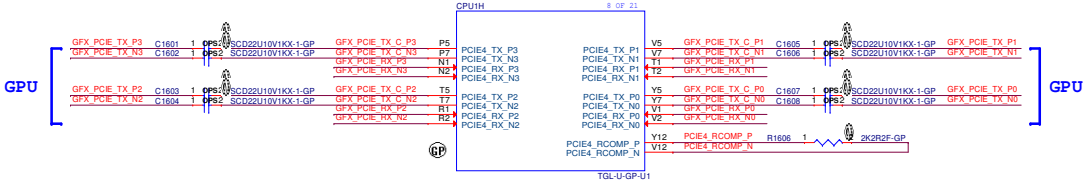
[71] PCH_TBT_PERST#

[71,72] TBT_FORCE_PWR

MM

[21] MEM_DIE_CFG





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)

Size: A2 | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 16 of 106

SSID = PCH

[61,63,71,76,91] PCH_PLTRST#
[91] SIO_SLP_S0#
[40,53,55] SIO_SLP_S3#
[40,92] SIO_SLP_S4#
[24,25,45] 3V_5V_PWRGD
[24] SIO_PWRBTN#
[24,40,64] PCH_RSMRST#
[24,26] IMVP_VR_ON
[24] SYS_PWROK
[40] SIO_SLP_SUS#
[40] VCCST_OVERRIDE
[40] CPU_C10_GATE#
[24] PCH_DPWROK
[44] AC_IN#
[24,40,44,46] ALL_SYS_PWRGD
[44,46] PWR_VCORE_VR_READY
[61] PCIE_WAKE#

Type-C BB

[72] TBT_PD_ALERT#
[91] TPM_SEL
[24,40,50] VCCIN_AUX_PWRGD
[24,71] TCP1_RETIMER_PERST_R_N
[24] EC_RESET#

CPU1L — 12 OF 21

SIO_SLP_SUS# DV49 — SLP_SUS#
SIO_SLP_S5# DM43 — GPD10/SLP_S5#
SIO_SLP_S4# DJ41 — GPD5/SLP_S4#
SIO_SLP_S3# DJ43 — GPD4/SLP_S3#
SIO_SLP_A# DM41 — GPD6/SLP_A#
DT44 — GPD9/SPL_WLAN#
SIO_SLP_S0# DD42 — GPP_B12/SLP_S0#
DN39 — SLP_LAN#
PM_RSMRST# DM35 — RSMRST#
SYS_RESET# DD10 — SYS_RESET#
PCH_PLTRST# DD41 — GPP_B13/PLTRST#
DSW_PWROK_R DK35 — DSW_PWROK
SYS_PWROK DF10 — SYS_PWROK
PCH_PWROK DN35 — PCH_PWROK
RTC_INTRUDER# DM37 — INTRUDER#
SPI_VCC_SEL DT49 — SPIVCCIOSEL
TGL-U-GP-U1

DM43: SIO_SLP_S5#
DR41: SIO_SLP_A#
DT44: SIO_SLP_WLAN#

TP1705 TP1707 TP1709

PROCPWRGD BM9 — TP_VCORE_PWRGD — TP1702 (follow 612304 Ver0.9)
GPD3/PWRBTN# DK41 — SIO_PWRBTN#
GPD0/BATLOW# DN41 — PCH_BATLOW#
GPD1/ACPRESENT DK43 — AC_PRESENT
GPP_B11/PMCALERT# CW40 — TBT_PD_ALERT#
GPP_H18/CPU_C10_GATE# DN27 — CPU_C10_GATE#
GPP_H3/SX_EXIT_HOLDOFF# DG31 — TPM_SEL
WAKE# DK39 — PCIE_WAKE#
GPD2/LAN_WAKE# DM41 DT41 — DM41: LAN_WAKE#
GPD11/LANPHYPC/DSWLDO_MON
GPD7 DN43 — GPD7_R — R1748 1 DY 2 0R2J-2-GP — TCP1_RETIMER_PERST_R_N
VCCSTPWRGOOD_TCSS CE5 — VCCSTPWRGOOD_TCSS — R1731 1 2 0R0402-PAD — VCCST_OVERRIDE
VCCST_PWRGD BP8 — VCCST_PWRGD_R
VCCST_OVERRIDE BP9 — VCCST_OVERRIDE_R — R1728 1 2 0R0402-PAD — VCCST_OVERRIDE
GPP_F20/EXT_PWR_GATE# DR12
GPP_F21/EXT_PWR_GATE2# DW12
DR12: EXT_PWR_GATE#
DW12: EXT_PWR_GATE2#

NON-G3

PCH_DPWROK — R1723 1 — 0R2J-2-GP — DSW_PWROK_R
ALL_SYS_PWRGD — D1704K — LRB520S-30T1G-GP — SYS_PWROK
PWR_VCORE_VR_READY — R1745 2 — 0R0402-PAD — PCH_PWROK
IMVP_VR_ON — R1746 2 — 0R0402-PAD

083.52030.008F
2ND = 83.R2003.A8M

D1701 LRB520S-30T1G-GP
083.52030.008F
2ND = 83.R2003.A8M

3D3V_AUX_S5 — R1737 1 — 100KR2J-1-GP — PM_RSMRST#_M
Q1702 2N7002KDW-1-GP
AC_IN# — AC_PRESENT — PM_RSMRST#
75.27002.F7C

SPI SELECT STRAP
Cap LOW → 3.3V
Cap DY → 1.8V

RTC_AUX_S5 — R1704 1MR2F-GP — RTC_INTRUDER#
R1714 DY 1MR2F-GP — C1701 SCD1U16V2KX-3DLGP

SPI SELECT STRAP
LOW → 3.3V
HIGH → 1.8V

3D3V_S5_VCCPRIM — R1705 DY 4K7R2J-2-GP — SPI_VCC_SEL
R1706 4K7R2J-2-GP

3D3V_S0 — R1701 1 — 10KR2J-3-GP — SYS_RESET#
3D3V_S5_VCCPRIM — R1713 1 — 100KR2J-1-GP — AC_PRESENT
R1715 1 — 10KR2J-3-GP — PCH_BATLOW#
3D3V_S5 — R1716 1 — 1KR2F-3-GP — PCIE_WAKE#

VCCST_OVERRIDE — R1730 — 100KR2J-1-GP
PCH_PWROK — R1732 — 100KR2J-1-GP
SYS_PWROK — R1733 — 100KR2J-1-GP
PCH_PLTRST# — R1744 — 100KR2J-1-GP
From PDG Request

3V_5V_PWRGD — R1729 1 — 68KR2J-GP — DSW_PWROK_R
DY — C1703 SCD1U16V2KX-3DLGP DY

VCCIN_AUX_PWRGD — R1747 1 — 68KR2J-GP — PM_RSMRST#
DY — C1704 SCD1U16V2KX-3DLGP DY

Volatge Level 1V

3D3V_S5 — C1702 SCD1U16V2KX-3DLGP
1D05V_VCCST — R1702 1KR2F-3-GP
U1701 74LVC1G07GW-GP
ALL_SYS_PWRGD — NC#1 VCC A GND Y — VCCST_PWRGD_RR — R1703 1 — 60D4R2F-GP — VCCST_PWRGD_R
73.01G07.0HG
2ND = 073.7SZ07.000G
3RD = 73.01G07.AHG

3D3V_AUX_S5 — R1708 10KR2J-3-GP — R1707 1 — 100KR2J-1-GP
Q1701 2N7002KDW-1-GP
3V_5V_POK# — 3V_5V_POK_C — R1710 1
PM_RSMRST# — R1709 1 DY 1KR2J-1-GP — PCH_RSMRST#
0R0402-PAD-7-NP-GP — 3V_5V_PWRGD
R1711 100KR2J-1-GP

20191224
follow Internal review
SCD1U16V2KX-3DLGP — C1714 — 3D3V_S5
U1703 SLG4E43789VTR-1-GP
PCH_RSMRST# — VDD — 3V_5V_PWRGD
PCH_DPWROK — PCH_RSMRST# — NC#7 — EC_PCH_SPI_EN
3D3V_S5_R — PCH_DPWROK — GND
DSW_PWROK
R1772 — 3V_5V_PWRGD_U1 — 3V_5V_PWRGD
R1774 — EC_PCH_SPI_EN_R 1 — EC_RESET#
R1775 R1771 R1773 — 0R0402-PAD-7-NP-GP
20191213
Follow HC ICL for G3 sharing
20191223
Change Part number
074.43789.M001

Power on sequence for G3 sharing

3D3V_S5 — 3D3V_S5_VCCPRIM — R1738 390KR2J-GP — 3D3V_S5_PCH_R
R1721 1 — 100KR2J-1-GP — 3D3V_S5_R
C1713 SCD1U16V2KX-3DLGP
U1710 74LVC1G08GW-1-GP
3D3V_S5 — B A VCC GND Y
73.01G08.L04
2ND = 073.7SZ08.000G
3RD = 73.01G08.IHG
DSW_PWROK_R — C1712 SCD1U16V2KX-3DLGP
R1734 1 — 0R0402-PAD
Q1703 2N7002KDW-1-GP
Q1703_2_3 — R1735 DY 1 — 100KR2J-1-GP
75.27002.F7C
R1736 DY 10KR2F-2-GP
DSW_PWROK
R1739 100KR2J-1-GP
R1776 1 DY 2 0R2J-2-GP

3D3V_S5_R — D1702 RB520S30-GP — PCH_DPWROK
83.R2003.A8M
2nd = 083.52030.008F

DSW_PWROK_R — D1703 RB520S30-GP — PCH_DPWROK
83.R2003.A8M
2nd = 083.52030.008F

PCH_RSMRST# — U1702 74LVC1G08GW-1-GP
DSW_PWROK — B A VCC GND Y — PM_RSMRST#
73.01G08.L04
2ND = 073.7SZ08.000G
3RD = 73.01G08.IHG

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PMU)
Size: Custom
Document Number: NAKIA_SHURI_N7_TGL-U
Rev: A00
Date: Wednesday, August 05, 2020
Sheet 17 of 106

SSID = PCH

[24,25,91] SPI0_CLK_CPU
[15,24,25] SPI0_HOLD_CPU
[15,24,25] SPI0_WP_CPU
[24,25,91] SPI0_SO_CPU
[24,25,91] SPI0_SI_CPU
[24,25] SPI0_CS_CPU_N0

SPI ROM
EC

[24,68] ESPI_CPU_IO0
[24,68] ESPI_CPU_IO1
[24,68] ESPI_CPU_IO2
[24,68] ESPI_CPU_IO3
[24,68] ESPI_CPU_CS#
[24,68] ESPI_CPU_RST#
[24,68] ESPI_CPU_CLK

WLAN

[61] WLAN_CLK_CPU_P
[61] WLAN_CLK_CPU_N
[61] CLK_PCIE_WLAN_REQ#

M.2 SSD

[63] SSD_CLK_CPU_N
[63] SSD_CLK_CPU_P
[63] CLK_PCIE_NVME_REQ#
[64] SATA_LED#

GPU

[76] GFX_CLK_CPU_N
[76] GFX_CLK_CPU_P
[76] CLK_PCIE_PEG_REQ#

[79,86] GC6_FB_EN
[76] DGPU_HOLD_RST#

XDP

SMBUS

[71] SML0_SMBCLK
[71] SML0_SMBDATA
[72] SML1_SMBCLK
[72] SML1_SMBDATA
[24,26,79] SML1_SMBCLK_THM
[24,26,79] SML1_SMBDATA_THM

OTHER

[24,61] SUSCLK

HW STRAP

[15] SML0_ALERT#
[15] GPP_E6
[15] GPP_E10
[15] GPP_E11

MEMORY

[20] MEM_CHA_EN
[21] MEM_SPEED_SEL

SD

[66] HOST_SD_WP#

TPM

[91] SPI0_CS_CPU_N2

CPU1E — 5 OF 21 — TGL-U-GP-U1

SPI0_CLK_CPU — R1826 — 22R2J-2-GP — SPI0_CLK_R_CPU — DJ37 SPI0_CLK
SPI0_HOLD_CPU — R1827 — 22R2J-2-GP — SPI0_HOLD_R_CPU — DG35 SPI0_IO3
SPI0_WP_CPU — R1828 — 22R2J-2-GP — SPI0_WP_R_CPU — DG39 SPI0_IO2
SPI0_SO_CPU — R1829 — 22R2J-2-GP — SPI0_SO_R_CPU — DJ33 SPI0_MISO
SPI0_SI_CPU — R1830 — 22R2J-2-GP — SPI0_SI_R_CPU — DJ35 SPI0_MOSI
DF35 SPI0_CS1#
SPI0_CS_CPU_N0 — DG37 SPI0_CS0#
SPI0_CS_CPU_N2 — DF39 SPI0_CS2#

GPP_E11 — DJ6 GPP_E11/SPI1_CLK/THC0_SPI1_CLK
DN5 GPP_E2/SPI1_IO3/THC0_SPI1_IO3
DR9 GPP_E1/SPI1_IO2/THC0_SPI1_IO2
DM6 GPP_E12/SPI1_MISO_IO1/THC0_SPI1_IO1
DK6 GPP_E13/SPI1_MOSI_IO0/THC0_SPI1_IO0
GPP_E10 — DK8 GPP_E10/SPI1_CS#/THC0_SPI1_CS#
SATA_LED# — DV11 GPP_E8/SPI1_CS1#/SATA_LED#
DGPU_HOLD_RST# — DW9 GPP_E17/THC0_SPI1_INT#
GPP_E6 — DT8 GPP_E6/THC0_SPI1_RST#
GC6_FB_EN — DN15 GPP_F11/THC1_SPI2_CLK
DK13 GPP_F15/GSXSRESET#/THC1_SPI2_IO3
DM13 GPP_F14/GSXDIN/THC1_SPI2_IO2
HOST_SD_WP# — DN13 GPP_F13/GSXSLOAD/THC1_SPI2_IO1
DJ15 GPP_F12/GSXDOUT/THC1_SPI2_IO0
DK15
MEM_CHA_EN — DN10 GPP_F16/GSXCLK/THC1_SPI2_CS#
DV14 GPP_F18/THC1_SPI2_INT#
GPP_F17/THC1_SPI2_RST#

DH3 CL_CLK
DH4 CL_DATA
DF2 CL_RST#

GPP_C0/SMBCLK — DK21 CPU_SMB_SCL — XDP
GPP_C1/SMBDATA — DM19 CPU_SMB_SDA
GPP_C2/SMBALERT# — DN19 CPU_SMB_ALERT#
GPP_C3/SML0CLK — DK19 SML0_SMBCLK — BB (TBT)
GPP_C4/SML0DATA — DM17 SML0_SMBDATA
GPP_C5/SML0ALERT# — DN17 SML0_ALERT#
GPP_C6/SML1CLK — DK17 SML1_SMBCLK — PD I2C2S_I2C
GPP_C7/SML1DATA — DJ17 SML1_SMBDATA
GPP_B23/SML1ALERT#/PCHHOT#/GSPI1_CS1# — CY50 SML1_ALERT# — TP1801
GPP_A5/ESPI_CLK — DN53 PCH_ESPI_CLK — R1804 — 33R2F-3-GP — ESPI_CPU_CLK
GPP_A3/ESPI_IO3/SUSACK# — DJ53 PCH_ESPI_IO3 — R1808 — 15R2F-2-GP — ESPI_CPU_IO3
GPP_A2/ESPI_IO2/SUSWARN#_SUSPWRDNACK — DH50 PCH_ESPI_IO2 — R1807 — 15R2F-2-GP — ESPI_CPU_IO2
GPP_A1/ESPI_IO1 — DP50 PCH_ESPI_IO1 — R1806 — 15R2F-2-GP — ESPI_CPU_IO1
GPP_A0/ESPI_IO0 — DP52 PCH_ESPI_IO0 — R1805 — 15R2F-2-GP — ESPI_CPU_IO0
GPP_A4/ESPI_CS# — DK52 ESPI_CS# — R1809 — ESPI_CPU_CS#
GPP_A6/ESPI_RESET# — DL50 ESPI_RESET# — R1810 — ESPI_CPU_RST#
R1814 — 75KR2J-GP
0R0402-PAD-7-NP-GP
0R0402-PAD-7-NP-GP
to EC,debug14pin

3D3V_S0 — RN1803 — CPU_SMB_SCL / CPU_SMB_SDA — SRN1KJ-7-GP
3D3V_S5 — RN1807 — SML0_SMBDATA / SML0_SMBCLK / SML1_SMBCLK / SML1_SMBDATA — SRN1KJ-7-GP
1D8V_S5 — R1823 — 10KR2J-3-GP — CPU_SMB_ALERT#
R1824 — 10KR2J-3-GP

RN1808 — SML0_SMBCLK / SML0_SMBDATA — SML1_SMBCLK_THM / SML1_SMBDATA_THM — SRN0J-6-GP

R1801 10KR2J-3-GP — DGPU_HOLD_RST# — OPS

CPU1K — 11 OF 21 — TGL-U-GP-U1

M.2 SSD — SSD_CLK_CPU_P / SSD_CLK_CPU_N — BW4 / BW5 — CLKOUT_PCIE_P4 / CLKOUT_PCIE_N4
CL7 / CL8 — CLKOUT_PCIE_P3 / CLKOUT_PCIE_N3
CB4 / CB5 — CLKOUT_PCIE_P2 / CLKOUT_PCIE_N2
WLAN — WLAN_CLK_CPU_P / WLAN_CLK_CPU_N — BY4 / BY3 — CLKOUT_PCIE_P1 / CLKOUT_PCIE_N1
GPU Gen4 — GFX_CLK_CPU_P / GFX_CLK_CPU_N — CN7 / CN8 — CLKOUT_PCIE_P0 / CLKOUT_PCIE_N0
R1819 — 60D4R2F-GP — XCLK_BIASREF — DJ5 XCLK_BIASREF
BW1 / BW2 — CLKOUT_PCIE_P6 / CLKOUT_PCIE_N6
CB2 / CB1 — CLKOUT_PCIE_P5 / CLKOUT_PCIE_N5

GPP_F19/SRCCLKREQ6# — DU14 — DF23 MEM_SPEED_SEL
GPP_H11/SRCCLKREQ5# — DG25 CLK_PCIE_NVME_REQ#
GPP_H10/SRCCLKREQ4# — DT24
GPP_D8/SRCCLKREQ3# — DT30
GPP_D7/SRCCLKREQ2# — DV30 CLK_PCIE_WLAN_REQ#
GPP_D6/SRCCLKREQ1# — DW30 CLK_PCIE_PEG_REQ#
GPP_D5/SRCCLKREQ0#
XTAL_OUT — DM1 XTL_38D4M_X2_CPU
XTAL_IN — DL1 XTL_38D4M_X1_CPU
GPD8/SUSCLK — DW41 SUSCLK
RTCX2 — DT47 XTL_32K_X2_CPU
RTCX1 — DR47 XTL_32K_X1_CPU
RTCRST# — DN37 RTC_RST#
SRTCRST# — DK37 SRTC_RST#

3D3V_S0 — RN1805 — CLK_PCIE_WLAN_REQ# / CLK_PCIE_NVME_REQ# / CLK_PCIE_PEG_REQ# — SRN10KJ-8-GP

RTC_AUX_S5 — RN1802 — SRN20KJ-1-GP — SRTC_RST# / RTC_RST#
C1803 SC1U10V2KX-1DLGP — G1801 GAP-OPEN — C1804 SC1U10V2KX-1DLGP

XTL_32K_X2_CPU / XTL_32K_X1_CPU — R1811 — 10MR2J-L-GP — C1802 — X1801 XTAL-32D768KHZ-88-GP — C1801
082.30003.0191
2ND = 082.30003.0301
SC15P50V2JN-DL-GP

XTL_38D4M_X2_CPU — R1831 0R2J-2-GP — XTL_38D4M_X2_CPU_R1
XTL_38D4M_X1_CPU — R1832 0R2J-2-GP — XTL_38D4M_X1_CPU_R1
R1820 — 200KR2F-L-GP — X1802
C1806 — XTAL-38D4MHZ-35-GP — C1805
082.30040.0221
SC12P50V2JN-DL-GP

Layout: Place at the open door area.
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SPI/LPC/SMBS/XTAL/CLK)
Size: A3 | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00
Date: Wednesday, August 05, 2020 | Sheet 18 of 106

SSID = PCH

Audio
[27] HDA_SYNC_CODEC
[27] HDA_BITCLK_CODEC
[27] HDA_SDOUT_CODEC
[27] HDA_SDI0
[15] HDA_SDO
[55] DMIC_PCH_CLK
[55] DMIC_PCH_DATA

GPU
[24,85] DGPU_PWROK
[86] DGPU_PWR_EN

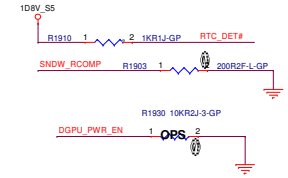
G SENSOR
[70] FFS_INT2

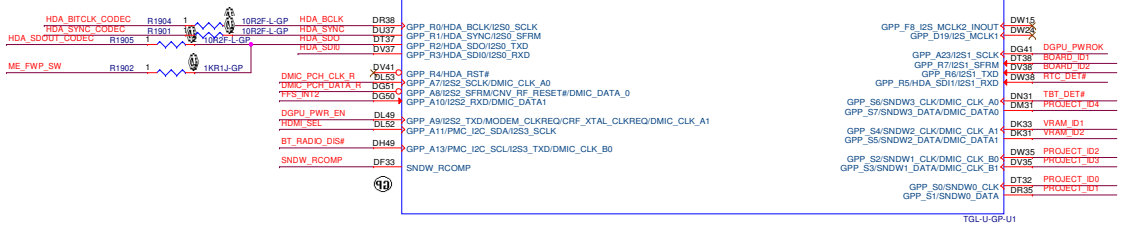
RTC
[25] RTC_DET#

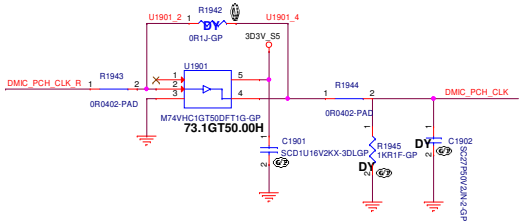
BT
[61] BT_RADIO_DIS#

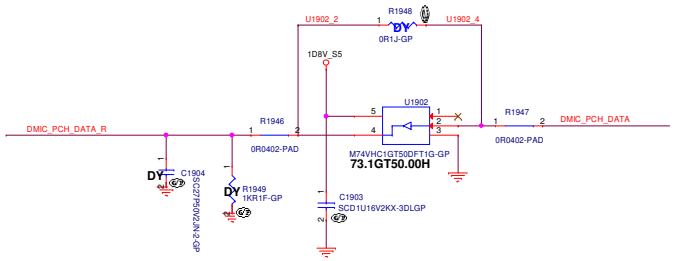
ME
[98] ME_FWP_SW

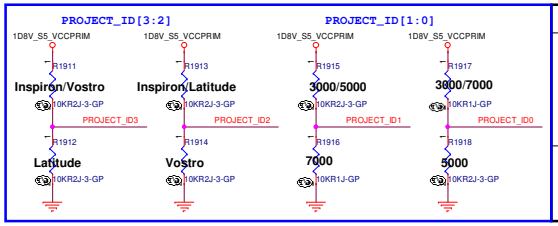
HDMI
[57] HDMI_SEL



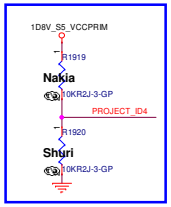




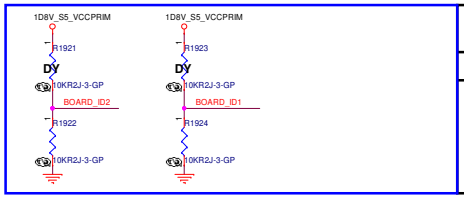




ID	Description	Setting	Mapping
PROJECT_ID[3:2]	Project Type	11	Inspiron
		10	Vostro
		01	Latitude Reseved
		00	N/A
PROJECT_ID[1:0]	Project Series	11	3000 Sereis
		10	5000 Sereis
		01	7000 Sereis
		00	N/A

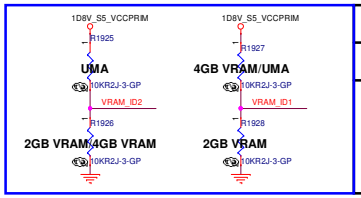


ID	Description	Setting	Mapping
PROJECT_ID4	Nakia/Shuri	1	Nakia
		0	Shuri



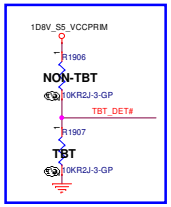
CY19 Board ID Mapping table

ID	Description	Setting	Mapping
Board ID[2:1]	Board SKU ID	11	N/A
		10	N/A
		01	TGL-UP4
		00	TGL-UP3



CY19 VRAM ID Mapping table

ID	Description	Setting	Mapping
VRAM_ID[2:1]	dGPU VRAM size	11	UMA Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM



ID	Description	Setting	Mapping
TBT_DET#	TBT function detected	1	Non-TBT
		0	TBT

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)

Size: A2 | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 19 of 106

SSID = PCH

TOUCH PAD/E3

[65,66] PCH_I2C1_SCL_TP
[65,66] PCH_I2C1_SDA_TP

G SENSOR

[70] FFS_INT1
[70] ISH_I2C0_ACC_SCL
[70] ISH_I2C0_ACC_SDA
[70] ISH_ACC1_INT#
[70] ISH_ACC2_INT#

AUDIO

[27] SPKR

KEYBOARD

[65] KB_LED_BL_DET

OTHER

[24] TABLE_MODE#
[24] NB_MODE#

MEMORY

[18] MEM_CHA_EN

PCH to Type-C PD

eDP

[55] DBC_PANEL_EN

LID

[24,67,92] ISH_LID_CL#_NB

UART

[68] UART2_TXD
[68] UART2_RXD

[91] TPM_SPI_IRQ#

PCH to BB

[71] I2C5_SCL
[71] I2C5_SDA

CPU1F

6 OF 21

MEM_CHB_EN — DC53 GPP_B16/GSPI0_CLK
DA51 GPP_B18/GSPI0_MOSI
DC49 GPP_B17/GSPI0_MISO
SPKR — DC50 GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#
DC52 GPP_B15/GSPI0_CS0#
TPM_SPI_IRQ# — CY49 GPP_B20/GSPI1_CLK
GC6_THM_DIS#_PCH — CY53 GPP_B22/GSPI1_MOSI
CY52 GPP_B21/GSPI1_MISO
DA50 GPP_B19/GSPI1_CS0#
TP2010 1
DV21 GPP_C9/UART0_TXD
FFS_INT1 — DT21 GPP_C8/UART0_RXD
DR21 GPP_C11/UART0_CTS#
DW21 GPP_C10/UART0_RTS#
DV19 GPP_C13/UART1_TXD/ISH_UART1_TXD
DT19 GPP_C12/UART1_RXD/ISH_UART1_RXD
DR18 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
DU19 GPP_C14/UART1_RTS#/ISH_UART1_RTS#

UART2_TXD — R2004 1 2 0R0402-PAD UART2_TXD_R — DJ21 GPP_C21/UART2_TXD
UART2_RXD — R2005 1 2 0R0402-PAD UART2_RXD_R — DG23 GPP_C20/UART2_RXD
DJ19 GPP_C23/UART2_CTS#
DF21 GPP_C22/UART2_RTS#

DV18 GPP_C17/I2C0_SCL
DW18 GPP_C16/I2C0_SDA

PCH to Touch Pad / E3 — PCH_I2C1_SCL_TP — DJ23 GPP_C19/I2C1_SCL
SDA/SCL/INT Pull UP on TP side(page65) — PCH_I2C1_SDA_TP — DT18 GPP_C18/I2C1_SDA

PCH to Type-C PD — TP2011 1TBT_I2C_SCL — DJ29 GPP_H5/I2C2_SCL
TP2012 1TBT_I2C_SDA — DJ31 GPP_H4/I2C2_SDA
SDA/SCL/INT Pull UP on PD side(page72) — DBC_PANEL_EN — DF29 GPP_H7/I2C3_SCL
DG29 GPP_H6/I2C3_SDA
DF25 GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
DF27 GPP_H8/I2C4_SDA/CNV_MFUART2_RXD

TGL-U-GP-U1

GPP_D14/ISH_UART0_TXD — DR27
GPP_D13/ISH_UART0_RXD — DW22
GPP_D16/ISH_UART0_CTS# — DV25 — KB_LED_BL_DET_R 1 — R2003 — 2KB_LED_BL_DET
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT5 — DT25
0R0402-PAD
GPP_B6/ISH_I2C0_SCL — DB45 ISH_I2C0_ACC_SCL
GPP_B5/ISH_I2C0_SDA — DB44 ISH_I2C0_ACC_SDA
3D3V_S0 — RN2025 SRN2K2J-1-GP
GPP_B8/ISH_I2C1_SCL — CY39
GPP_B7/ISH_I2C1_SDA — DB47
Accelerometer sensor
GPP_B10/I2C5_SCL/ISH_I2C2_SCL — DD47 I2C5_SCL
GPP_B9/I2C5_SDA/ISH_I2C2_SDA — DD44 I2C5_SDA
GPP_E16/ISH_GP7 — DJ8
GPP_E15/ISH_GP6 — DR7
GPP_D18/ISH_GP5 — DR24 ISH_LID_CL#_NB
GPP_D17/ISH_GP4 — DU25
GPP_D3/ISH_GP3/BK3/SBK3 — DV31
GPP_D2/ISH_GP2/BK2/SBK2 — DU31 ISH_TABLE_MODE# — R2009 1 2 0R0402-PAD TABLE_MODE#
GPP_D1/ISH_GP1/BK1/SBK1 — DT27 ISH_ACC2_INT#
GPP_D0/ISH_GP0/BK0/SBK0 — DV27 ISH_ACC1_INT#
GPP_RCOMP — DR51 GPP_RCOMP — R2021 1 200R2F-L-GP
GPP_T3/I2C7_SCL — DN33
GPP_T2/I2C7_SDA — DT35
GPP_U5/GSPI3_CLK — DG17
GPP_U4/GSPI3_CS0# — DG19

R2002 1 10KR1J-GP NB_MODE#

1D8V_S5 — R2031 10KR2J-3-GP — MEM_CHA_EN — R2030 10KR2J-3-GP DY
1D8V_S5 — R2033 10KR2J-3-GP — MEM_CHB_EN — R2032 10KR2J-3-GP DY

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)
Size: A3
Document Number: NAKIA_SHURI_N7_TGL-U
Rev: A00
Date: Wednesday, August 05, 2020
Sheet 20 of 106

SSID = PCH

[61] CNV_WR_DN0
[61] CNV_WR_DP0
[61] CNV_WR_DN1
[61] CNV_WR_DP1
[61] CNV_WR_CLKN
[61] CNV_WR_CLKP
[61] CNV_WT_DN0
[61] CNV_WT_DP0
[61] CNV_WT_DN1
[61] CNV_WT_DP1
[61] CNV_WT_CLKN
[61] CNV_WT_CLKP
[61] CNV_BRI_RSP
[61] CNV_RGI_RSP
[15,61] CNV_RGI_DT
[61] CNV_BRI_DT
[61] BT_PCMFRM_RSTN
[61] BT_PCMOUT_CLKREQ0

MEMORY

[3] MEM_CONFIG4
[16] MEM_DIE_CFG1
[18] MEM_SPEED_SEL

CPU1J — 10 OF 21

D22 CSI_F_DP1
B22 CSI_F_DN1
E22 CSI_F_DP0
D20 CSI_F_DN0
A20 CSI_F_CLK_P
B20 CSI_F_CLK_N
B18 CSI_E_DP1/CSI_F_DP2
A18 CSI_E_DN1/CSI_F_DN2
D18 CSI_E_DP0/CSI_F_DP3
E18 CSI_E_DN0/CSI_F_DN3
C16 CSI_E_CLK_P
D16 CSI_E_CLK_N
D15 CSI_C_DP2
E15 CSI_C_DN2
A15 CSI_C_DP3
B15 CSI_C_DN3
L18 CSI_C_DP1
N18 CSI_C_DN1
L20 CSI_C_DP0
N20 CSI_C_DN0
G20 CSI_C_CLK_P
H20 CSI_C_CLK_N
H16 CSI_B_DP1
G16 CSI_B_DN1
G18 CSI_B_DP0
H18 CSI_B_DN0
L16 CSI_B_CLK_P
N16 CSI_B_CLK_N
G14 CSI_B_DP2
H14 CSI_B_DN2
L14 CSI_B_DP3
N14 CSI_B_DN3
K14 CSI_RCOMP

DK47 CNV_WT_DP1
DM47 CNV_WT_DN1
DN49 CNV_WT_DP0
DR49 CNV_WT_DN0
DN45 CNV_WT_CLKP
DN47 CNV_WT_CLKN
DU43 CNV_WR_DP1
DV43 CNV_WR_DN1
DR44 CNV_WR_DP0
DT43 CNV_WR_DN0
DV44 CNV_WR_CLKP
DW44 CNV_WR_CLKN
DN51 CNV_WT_RCOMP
DJ13 CNV_RGI_RSP
DG13 CNV_RGI_DT
DF15 CNV_BRI_RSP
DF17 CNV_BRI_DT
DJ10 CLKREQ_CNV
DV15
DK10 CNV_RF_RESET#

GPP_F3/CNV_RGI_RSP/UART0_CTS#
GPP_F2/CNV_RGI_DT/UART0_TXD
GPP_F1/CNV_BRI_RSP/UART0_RXD
GPP_F0/CNV_BRI_DT/UART0_RTS#
GPP_F5/MODEM_CLKREQ/CRF_XTAL_CLKREQ
GPP_F6/CNV_PA_BLANKING
GPP_F4/CNV_RF_RESET#

MEM_DIE_CFG0 DK25
MEM_CONFIG1 DM25
MEM_CONFIG2 DN25
MEM_CONFIG3 DJ25
DR30
GPP_H23/IMGCLKOUT4
GPP_H22/IMGCLKOUT3
GPP_H21/IMGCLKOUT2
GPP_H20/IMGCLKOUT1
GPP_D4/IMGCLKOUT_0/BK4/SBK4

TGL-U-GP-U1

1D8V_S5 — R2110 — 10KR2J-3-GP — **B1 CPU** — MEM_SPEED_SEL — R2111 — 10KR2J-3-GP — **B0 CPU**

R2103 1 — 150R2F-1-GP — CSI_RCOMP

R2102 1 — 150R2F-1-GP

R2104 1 — 33R2F-3-GP — BT_PCMOUT_CLKREQ0

R2105 1 — 33R2F-3-GP — BT_PCMFRM_RSTN

DRAM Support list

1.Micron:2FG92$CA IC,LP4X,16GB,4266,X32,16G,TGL MT53E512M32D2NP-046 WT:E DRAM 8G;DDP	2.Micron:K7HT2$CA IC,LP4X,32GB,4266,X32,16G,TGL IC SDRAM DDR4 32G MT53E1G32D2NP-046 WT:A DRAM 16G;DDP
GP 3.Samsung:15NY1$AA IC SDRAM LPDDR4X 16GB K4U6E3S4AA-MGCR DRAM 8G;SDP	4.Samsung:K7HT2$AA IC SDRAM LPDDR4X 32GB K4UBE3D4AA-MGCR DRAM 16G;SDP

MEM_CONFIG Mapping table

ID	Description	Setting	Mapping
MEM_CONFIG[4:3]	On-board memory configuration for chip vendor	11	DIMM Design
		10	Micron
		01	Hynix
		00	Samsung
MEM_CONFIG[2:1]	On-board memory configuration for total memory size per channel	11	N/A
		10	16GB
		01	8GB
		00	4GB

1D8V_S5 — R2112 — 10KR2J-3-GP — **Micron** — MEM_CONFIG4 — R2113 — 10KR2J-3-GP — **Samsung/Hynix**

1D8V_S5 — R2114 — 10KR2J-3-GP — **Hynix** — MEM_CONFIG3 — R2115 — 10KR2J-3-GP — **Samsung/Micron**

1D8V_S5 — R2116 — 10KR2J-3-GP — **16GB** — MEM_CONFIG2 — R2117 — 10KR2J-3-GP — **4GB/8GB**

1D8V_S5 — R2118 — 10KR2J-3-GP — **8GB** — MEM_CONFIG1 — R2119 — 10KR2J-3-GP — **4GB/16GB**

CY19 Board ID Mapping table

ID	Description	Setting	Mapping
MEM_Die CONFIG[1:0]	SDP/DDP/QDP/ODP Configuration	11	ODP
		10	QDP
		01	DDP
		00	SDP

1D8V_S5 — R2106 — 10KR2J-3-GP — **ODP/QDP** — MEM_DIE_CFG1 — R2107 — 10KR2J-3-GP — **SDP/DDP**

1D8V_S5 — R2108 — 10KR2J-3-GP — **ODP/DDP** — MEM_DIE_CFG0 — R2109 — 10KR2J-3-GP — **SDP/QDP**

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CSI/EMMC/CNVi)
Size: A3
Document Number: NAKIA_SHURI_N7_TGL-U
Rev: A00
Date: Wednesday, August 05, 2020
Sheet 21 of 106

SSID = PCH

[50] VCCAUX_SENSE
[50] VSSAUX_SENSE
[50] CORE_VID0
[50] CORE_VID1
[3,24,44,46] PROCHOT#_CPU
[40] VNN_CTRL_R
[40] V1P05_CTRL_R

CPU1N — 14 OF 21 — TGL-U-GP-U1

1D8V_VCCIN_AUX
AB12 AC10 AE10 AK2 AR10 AT12 AU10 AW10 BV1 BV39 BW40 BY39 CC1 CD12 CF10 CG12 CH10 CJ1 CJ12 CK10 CL12 CM10 CP1 CP10 CR12 CT10 CU12 CY1 AK1
VCCIN_AUX

PH/PL 100R at VR side.

VSSAUX_SENSE AV9 — VCCIN_AUX_VSSSENSE
VCCAUX_SENSE AT9 — VCCIN_AUX_VCCSENSE

(200mA) 1D05V_VNN_BYPASS
DD17 DD18 — VCC_VNNEXT_1P05

3D3V_S5_VCCPRIM (200mA) 1D05V_S5_BYPASS
DA15 DA17 — VCC_V1P05EXT_1P05

R2211 1 — 2 10KR2J-3-GP — VRALERT# DB39 — GPP_B2/VRALERT#
VNN_CTRL_R — R2212 1 — 2 0R0402-PAD — VNN_CTRL DV12 — GPP_F22/VNN_CTRL
V1P05_CTRL_R — R2213 1 — 2 0R0402-PAD — V1P05_CTRL DT12 — GPP_F23/V1P05_CTRL

CORE_VID0 DB37 — GPP_B0/CORE_VID0
CORE_VID1 DB38 — GPP_B1/CORE_VID1

PROCHOT#_CPU — A D2201 K — VRALERT#
LRB520S-30T1G-GP
083.52030.008F
2ND = 83.R2003.A8M

(1.3A) 1D8V_S5_VCCPRIM — RP2203 1 — 2 0R0805-PAD — 1D8V_S5
CY18 CY20 CY24 CY26 DA18 DA20 DA22 DA24 DA26 DC18 DC20 DC22 DC24 DC26 DD20 DD22 DV22 — VCCPRIM_1P8

(200mA) 3D3V_S5_VCCPRIM
DA35 DC28 DC30 DD30 — VCCPRIM_3P3

DV34 — DCPRTC — 3D3V_RTC_EXT
DV46 — VCCLDOSTD_0P85 — 0D85V_S5_VCCLDOSTD_OUT
DV16 DC15 — VCCA_CLKLDO_1P8 — 1D8V_S5_CLKLDO (165mA)
DV28 — VCCDPHY_1P24 — 1D24V_S5_VCCDPHY_OUT
DD38 — VCCDSW_1P05 — 1D05V_S5_VCCDSW_OUT
BR3 BR4 BT5 — VCC1P05 — 1D05V_S5_OUT (1.5A)

Supply to VCCST & VCCSTG

DA31 DC33 DC31 — VCCPRIM1P05_OUT_PCH — 1D05V_S5_VCCPRIM_OUT (Output)

VCCGPPR 3.3V or 1.8V

DC35 — VCCRTC — RTC_AUX_S5
DD37 — VCCDSW_3P3 — 3D3V_VCCDSW
DA28 — VCCGPPR — 1D8V_GPPR_S5

(3mA) R2202 0R2J-2-GP — 3D3V_S5
R2207 1 — 2 0R0402-PAD — 1D8V_S5

CY31 CY33 CV39 — VCCPRIM_3P3 — 3D3V_S5_VCCPRIM
1D8V_S5_VCCPRIM

AP12 — RSVD#AP12 — TP_VCCANA_EHV 1 — TP2201

Trace width > 40mil
1D05V_S5_VCCDSW_OUT — C2204 SC1U10V2KX-1DLGP

Place cap within 3mm from SOC edge
1D24V_S5_VCCDPHY_OUT — For CNV2 — C2205 SC4D7U6D3V2MX-1-GP

Place cap within 3mm from SOC edge
0D85V_S5_VCCLDOSTD_OUT — C2213 SC2D2U10V3KX-1DLGP-U

Must take care this power layout and add shield GND.
1D8V_S5 — R2204 1 — 2 0R0402-PAD — 1D8V_S5_CLKLDO (165mA)
C2215 SC22U6D3V3MX-1-DL-GP
C2216 SC22U6D3V3MX-1-DL-GP

PH Same as SPI Programming Guide for details
1D8V_S5 — RN2201 1 2 4 3 — CORE_VID0 CORE_VID1 — SRN10KJ-5-GP

(1.3A) 1D8V_S5_VCCPRIM — C2210 SC1U10V2KX-1DLGP — C2211 SC1U10V2KX-1DLGP
3D3V_S5_VCCPRIM — C2201 SC1U10V2KX-1DLGP — C2202 SCD1U16V2KX-3DLGP
RTC_AUX_S5 — C2206 SC1U10V2KX-1DLGP — C2207 SCD1U16V2KX-3DLGP
3D3V_RTC_EXT — C2248 SCD1U16V2KX-3DLGP
1D05V_S5_VCCPRIM_OUT — C2203 SC1U10V2KX-1DLGP

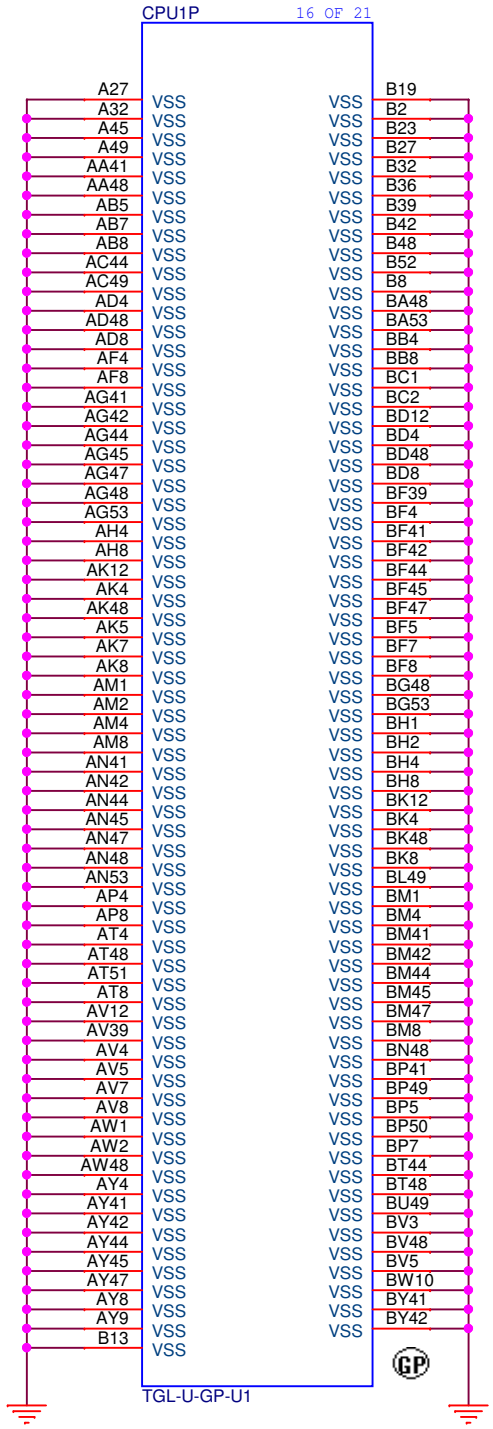
(200mA) 1D05V_S5_BYPASS — C2246 SC1U10V2KX-1DLGP
(200mA) 1D05V_VNN_BYPASS — C2247 SC1U10V2KX-1DLGP
1D05V_S5_OUT — C2208 SC1U10V2KX-1DLGP
3D3V_VCCDSW — C2209 SC1U10V2KX-1DLGP — Close to pin DD37
1D8V_GPPR_S5 — C2214 SCD1U16V2KX-3DLGP

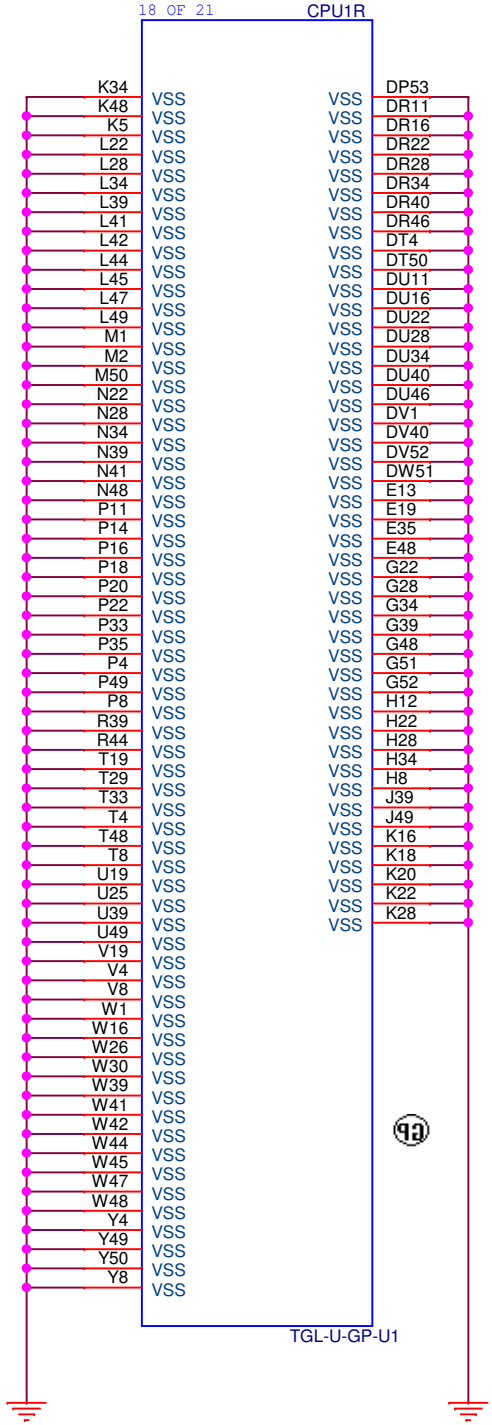
<Core Design>

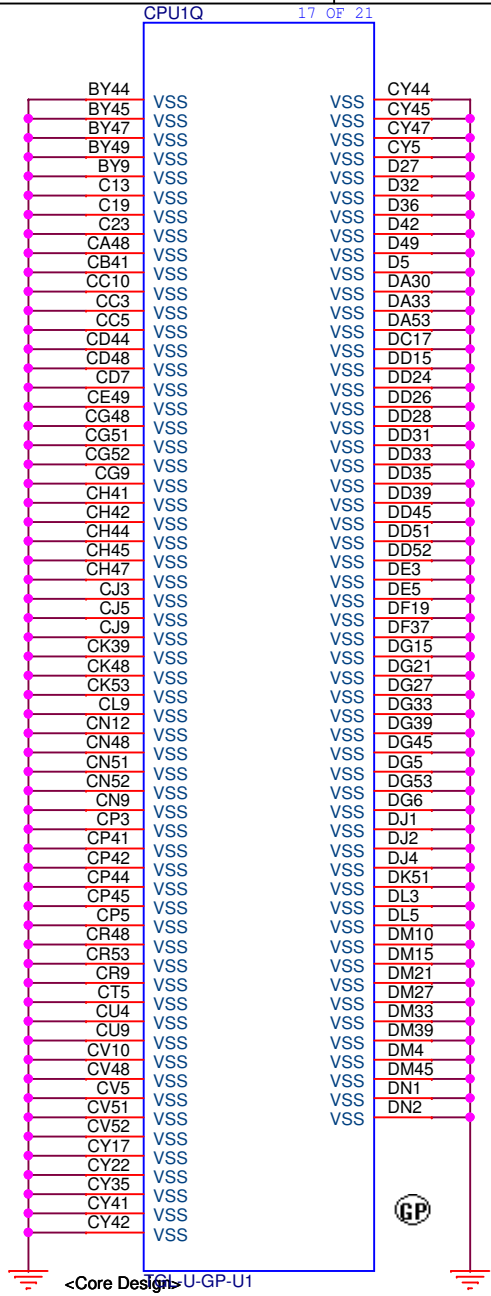
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCH-LP PWR&Caps)
Size: A3 | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00
Date: Wednesday, August 05, 2020 | Sheet 22 of 106

SSID = PCH







<Core Design>

DELL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 23 of 106

SSID = KBC

BOARD_ID VERSION A/D	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Nakia_X00	100.0K	10.0K	3.0V
Nakia_X01	100.0K	17.8K	2.801V
Nakia_X02	100.0K	27.0K	2.598V
Nakia_A00	100.0K	37.4K	2.402V
Nakia_X03	100.0K	49.9K	2.201V
Nakia_X04	100.0K	64.9K	2.001V
Nakia_X05	100.0K	82.5K	1.808V
Nakia_A01	100.0K	107K	1.594V
Nakia_A02	100.0K	154K	1.299V
Nakia_A03	100.0K	200K	1.100V

MODEL_ID_DET (GPIO15)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE	
Shuri_N7_ Nakia_N7_UMA_TBT	100.0K	10.0K	3.0V	63.10334.1DL
TBD	100.0K	17.8K	2.801V	
Shuri_N5_V5_N7_Nakia_N7_UMA_NO_TBT	100.0K	27.0K	2.598V	64.27025.6DL
TBD	100.0K	37.4K	2.402V	
Shuri_N5_V5_N7_Nakia_N7_DIS_NO_TBT	100.0K	49.9K	2.201V	64.49925.6DL
TBD	100.0K	64.9K	2.001V	
Shuri_N7_ Nakia_N7_DIS_TBT	100.0K	82.5K	1.808V	64.82525.6DL
TBD	100.0K	107K	1.594V	
TBD	100.0K	154K	1.299V	
TBD	100.0K	200K	1.100V	

EC to TBT/TP

BATTER /CHARGER
CPU/ Thermal/TYPEC

RTC GEN 9 reset circuit

Power Switch Logic(PSL)

Layout Note:

For eSPI

For G3 Flash Share

83.00355.G1F
2nd = 83.14148.01F
3RD = 83.00316.A1F

071.01515.0A03

75.00054.A7D
2nd = 75.00054.T7D

75.27002.F7C

20.K0460.010

<Core Design>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

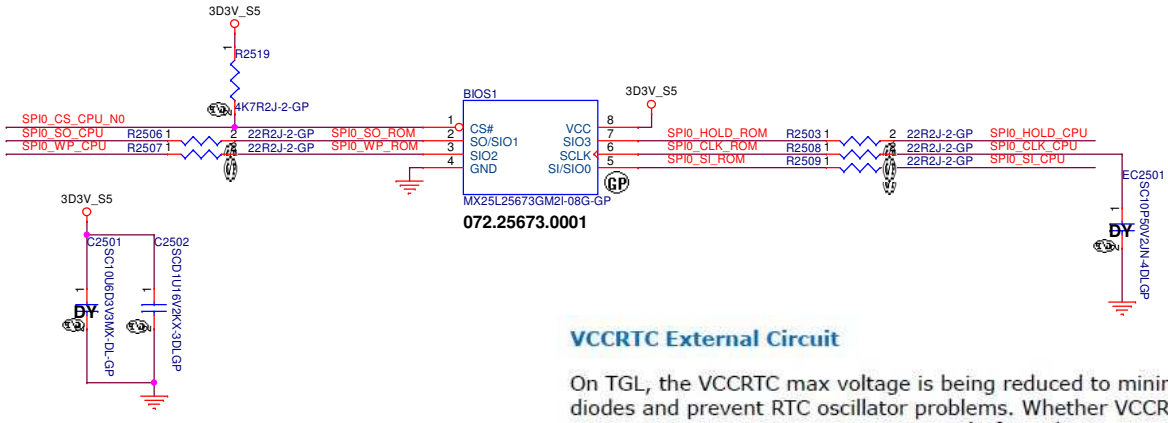
Title: **KBC Nuvoton MEC1515**

Size	Document Number	Rev
A3	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 24 of 156

Main Func = SPI Flash

[15,18,24,91] SPI0_SI_CPU
[18,24,91] SPI0_SO_CPU
[18,24,91] SPI0_CLK_CPU
[18,24] SPI0_CS_CPU_N0
[15,18,24] SPI0_WP_CPU
[15,18,24] SPI0_HOLD_CPU

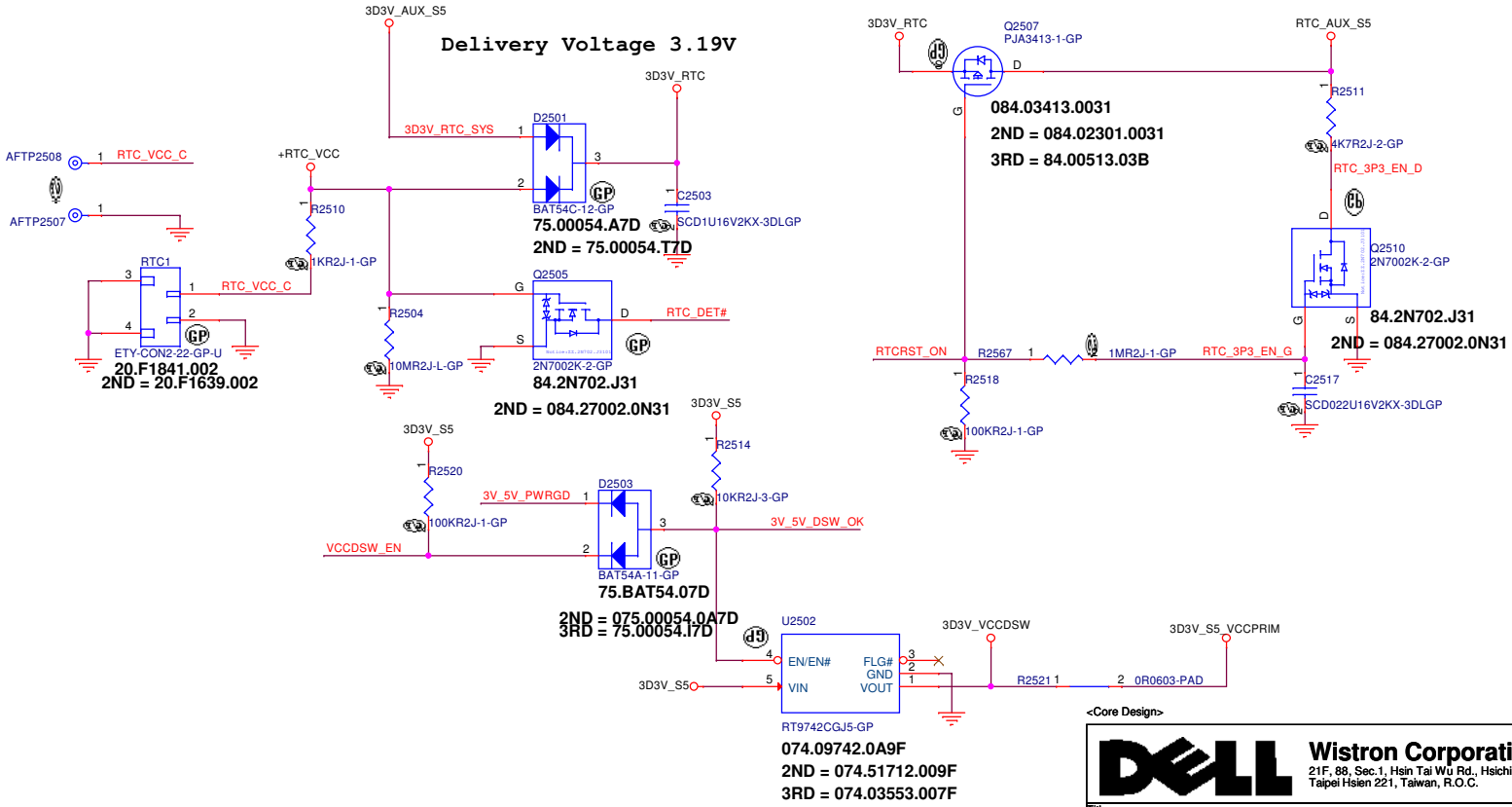


VCCRTC External Circuit

On TGL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.3V.

Main Func = RTC

[24] RTCRST_ON
[24] VCCDSW_EN
[17,24,45] 3V_5V_PWRGD
[19] RTC_DET#
[17,40] SIO_SLP_SUS#



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC
Size: A3
Document Number: NAKIA_SHURI_N7_TGL-U
Rev: A00
Date: Wednesday, August 05, 2020
Sheet 25 of 106

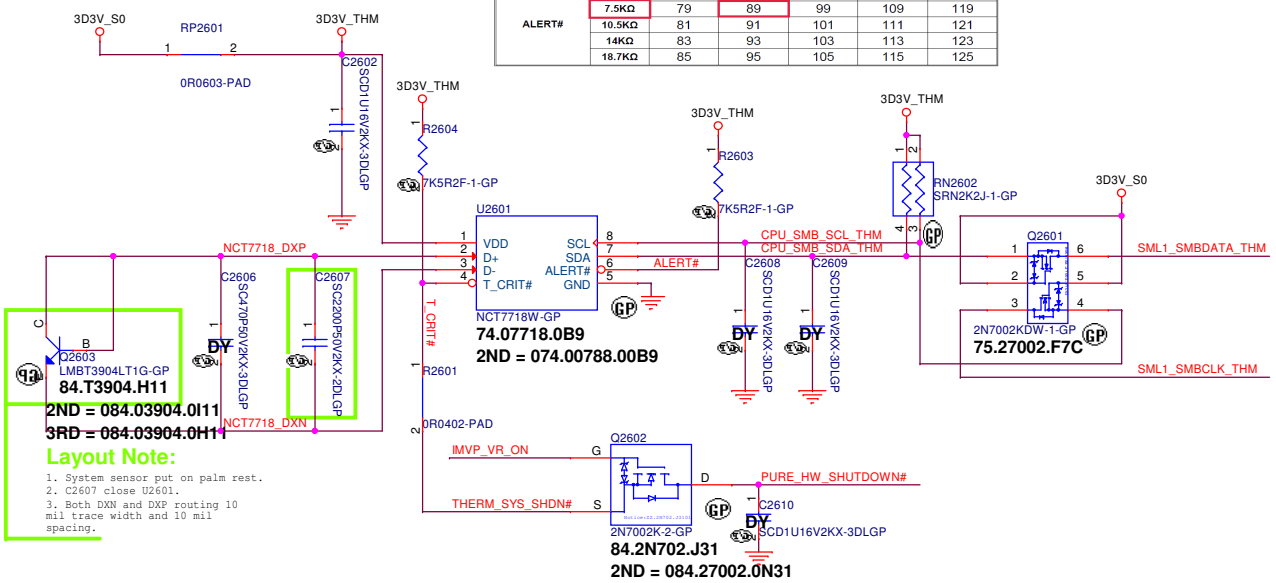
Main Func = Thermal Sensor

[18,24,79] SML1_SMBCLK_THM
[18,24,79] SML1_SMBDATA_THM

[17,24] IMVP_VR_ON

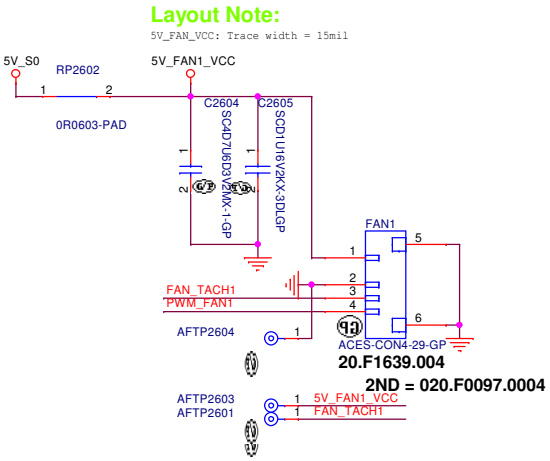
[40] PURE_HW_SHUTDOWN#

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



Main Func = Thermal Sensor

[24] PWM_FAN1
[24] FAN_TACH1



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size	Document Number	Rev
A3	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 26 of 106

Audio Codec Chip ALC3204

Main Func = Audio

[19] HDA_SDI0
[19] HDA_SDOUT_CODEC
[19] HDA_SYNC_CODEC
[19] HDA_BITCLK_CODEC

[29] AUD_SPK_R+
[29] AUD_SPK_R-

[29] AUD_SPK_L+
[29] AUD_SPK_L-

[55] DMIC_SCL_CODEC
[55] DMIC_SDA_CODEC

[66] AUD_SENSE
[24] NB_MUTE#
[20] SPKR
[24] BEEP
[29,66] AUD_RING
[29,66] AUD_SLEEVE

[29] LINE1_L
[29] LINE1_R

[29] LINE1_VREFO
[29] MIC2_VREFO_R

[29,66] AUD_HP1_JACK_L
[29,66] AUD_HP1_JACK_R

5V_S0 — RP2701 0R0805-PAD — +5V_PVDD
RP2702 0R0805-PAD

1D8V_S0 — RP2709 — 1D8V_CPVDD
0R0603-PAD

moat Analog Digital

1.8V power rail should be supplied by linear regulator, not awitching regulator.if switch regulator is unavilable, please make sure that switch frequency operates at out-band(over 20KHz)

1D8V_S0 — R2719 0R0402-PAD — C2710 SC10U6D3V3MX-DL-GP — AUD_AGND

+5V_PVDD >2A

C2713 SC10U6D3V3MX-DL-GP
C2714 SCD1U16V2KX-3DLGP
C2717 SC10U6D3V3MX-DL-GP
C2718 SCD1U16V2KX-3DLGP

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

AUD_SPK_L+
AUD_SPK_L-
AUD_SPK_R-
AUD_SPK_R+

NB_MUTE#

DVDD must >= DVDD_IO

1D8V_S0 — RP2715 — 1D8V_DVDD
0R0603-PAD
C2740 SC2D2U10V3KX-1DLGP-U
C2741 SCD1U16V2KX-3DLGP

SPKR
BEEP
D2703 BAT54C-12-GP
C2735 SCD1U16V2KX-3DLGP
AUD_PC_BEEP_C
AUD_PC_BEEP
R2739 1KR2J-GP
C2739 SC100P50V2JN-3DLGP
75.00054.A7D
2ND = 75.00054.17D

Open drain output. pull up to DVDD or max. 5V
For RTC Gen9 reset circuit change power rail. 20170921

3D3V_RTC — R2708 0R0402-PAD — V3D3_STB
3D3V_S0 — R2716 100KR2J-1-GP — DVSS

HDA_SDI0 — R2724 0R0402-PAD — HDA_CODEC_SDIN0
HDA_BITCLK_CODEC — R2723 22R2J-2-GP — HDA_BITCLK_CODEC_R

AUD_HP1_JACK_L
AUD_HP1_JACK_R

1D8V_CPVDD
C2705 SC2D2U10V3KX-1DLGP-U
C2704 SCD1U16V2KX-3DLGP
C2700 SC2D2U10V3KX-1DLGP-U
C2701 SC2D2U10V3KX-1DLGP-U
C2699 SC2D2U10V3KX-1DLGP-U

AUD_AGND
C2702 SC2D2U10V3KX-1DLGP-U
R2702 100KR2J-1-GP
C2703 SC2D2U10V3KX-1DLGP-U

U2701 ALC3204-CG-GP-U

30	CBP	31	AVSS2
29	CPVDD	32	LDO2-CAP
28	CBN	33	AVDD2
27	CPVEE	34	PVDD1
26	HP-OUT-R	35	SPK-L+
25	HP-OUT-L	36	SPK-L-
24	LINE1-VREFO-L	37	SPK-R-
23	MIC2-VREFO	38	SPK-R+
22	VREF	39	PVDD2
21	LDO1-CAP	40	PDB
		41	GND

C2711 SC10U6D3V3MX-DL-GP — LDO2_CAP — +3V_1D8V_AVDD

ALC3204
QFN40 (5X5)
071.03204.0003

2	DVDD	20	AVDD1
3	GPIO0/DMIC-DATA12	19	AVSS1
4	GPIO1/DMIC-CLK	18	LINE1-L
5	SDATA-OUT	17	LINE1-R
6	BIT-CLK	16	VD33STB
7	LDO3-CAP	15	MIC2-CAP
8	SDATA-IN	14	SLEEVE/MIC2-R
9	DVDD-IO	13	RING2/MIC2-L
10	SYNC	12	HP/LINE1-JD_JD1
	DC_DET	11	PCBEEP

LINE1_L
LINE1_R
V3D3_STB
MIC_CAP — C2715 SC10U6D3V3MX-DL-GP
AUD_SLEEVE
AUD_RING
AUD_HPJD_N
AUD_PC_BEEP

3D3V_S0 — RP2725 0R0603-PAD — DVDD_R
C2720 SC10U6D3V2MX-2-GP
C2721 SCD1U16V2KX-3DLGP
place close to pin1

1D8V_DVDD
C2723 SC4D7U6D3V2MX-1-GP
place close to pin8

C2722 SC10U6D3V3MX-DL-GP

DMIC_SDA_CODEC
DMIC_SCL_CODEC
HDA_SDOUT_CODEC
HDA_BITCLK_CODEC
LDO3_CAP
HDA_CODEC_SDIN0
HDA_SYNC_CODEC
SSA

Analog Digital moat

+5V_AVDD — moat RP2703 — 5V_S0
0R0603-PAD
C2707 SC10U6D3V2MX-DL-GP
C2706 SCD1U16V2KX-3DLGP
AUD_AGND

Layout Note:
Place close to Pin 20

3D3V_S0 — R2717 100KR2J-1-GP — NB_MUTE#
20180911 Vendor stuff

moat 20180904 EMC modify
EC2701 SC1KP50V2KX-1DLGP
EC2702 SC1KP50V2KX-1DLGP
EC2703 SC1KP50V2KX-1DLGP
EC2704 SC1KP50V2KX-1DLGP
EC2705 SC1KP50V2KX-1DLGP
AUD_AGND

3D3V_S0 — R2710 100KR2J-1-GP
AUD_SENSE — R2711 200KR2F-L-GP — AUD_HPJD_N

R2704 0R0603-PAD
R2705 0R0603-PAD
R2706 0R0603-PAD
AUD_AGND

Layout Note:
Tied at point only under Codec or near the Codec

Azalia I/F EMI
HDA_SDOUT_CODEC — EC2709 SC22P50V2JN-4DLGP
HDA_BITCLK_CODEC — EC2710 SC22P50V2JN-4DLGP
DMIC_SDA_CODEC — EC2711 SC22P50V2JN-4DLGP
DMIC_SCL_CODEC — EC2706 SC33P50V2JN-3DLGP
20180911 Vendor add

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3204
Size: A3
Document Number: NAKIA_SHURI_N7_TGL-U
Rev: A00
Date: Wednesday, August 05, 2020
Sheet 27 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	***NAKIA_SHURI_N7_TGL-U***	***A00***

Date: Wednesday, August 05, 2020 Sheet 28 of 106

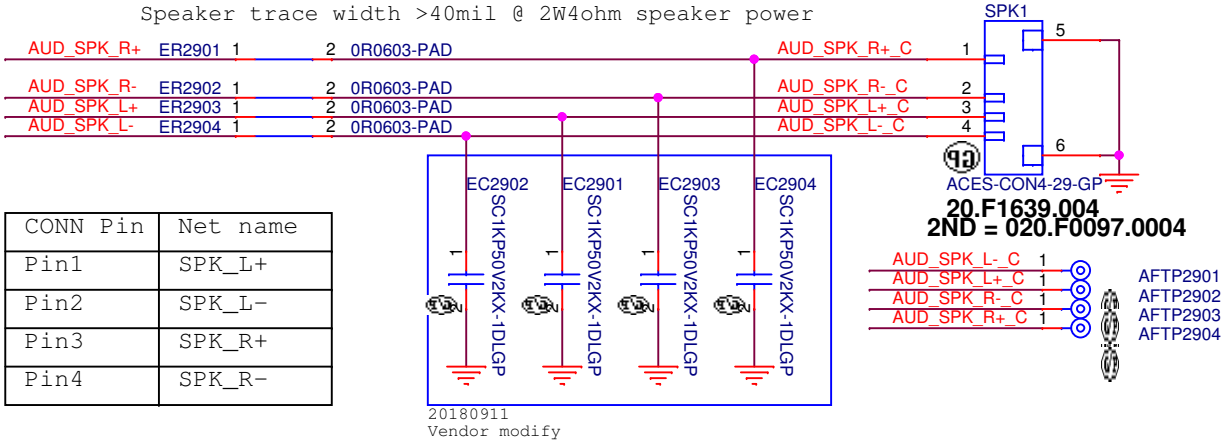
Main Func = Audio

[27] AUD_SPK_R+
[27] AUD_SPK_R-
[27] AUD_SPK_L-
[27] AUD_SPK_L+

Speaker

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

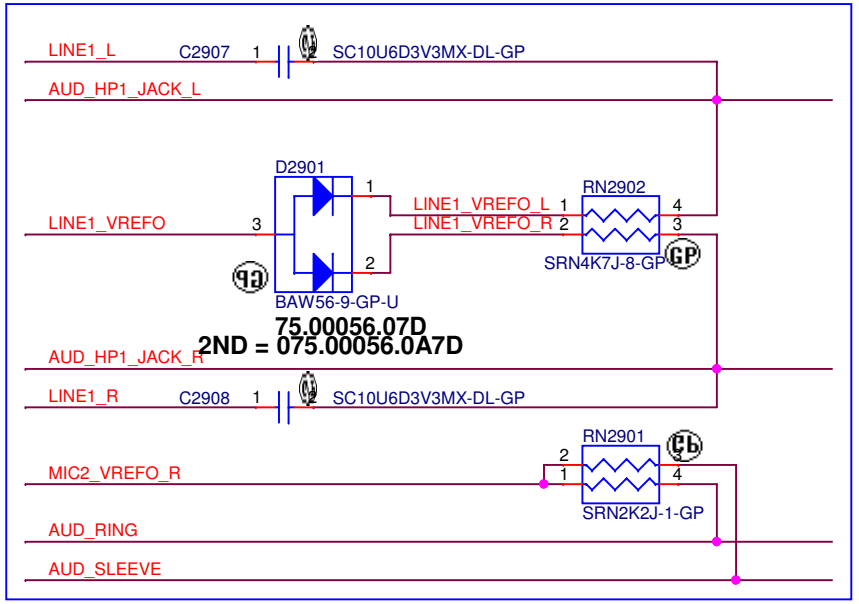


CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R+
Pin4	SPK_R-

20180911
Vendor modify

[27] LINE1_L
[27,66] AUD_HP1_JACK_L
[27] LINE1_VREFO
[27,66] AUD_HP1_JACK_R
[27] LINE1_R

[27] MIC2_VREFO_R
[27,66] AUD_SLEEVE
[27,66] AUD_RING



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio IO***

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 29 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 30 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN RTL8106

Size	Document Number	Rev
A4	***NAKIA_SHURI_N7_TGL-U***	***A00***

Date: Wednesday, August 05, 2020 Sheet 31 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

XFOM&RJ45

Size	Document Number	Rev
A4	***NAKIA_SHURI_N7_TGL-U***	***A00***

Date: Wednesday, August 05, 2020 Sheet 32 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CARDREADER (SDIO/SD Conn)

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 33 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	***NAKIA_SHURI_N7_TGL-U***	***A00***

Date: Wednesday, August 05, 2020 Sheet 34 of 106

Main Func = USB 3.1 Gen1

[16] USB1_USB31_TX_N
[16] USB1_USB31_TX_P
[16] USB1_USB31_RX_N
[16] USB1_USB31_RX_P

[16] USB1_USB20_N
[16] USB1_USB20_P

[16] USB_OC0#

[24,66] USB_PWR_EN#

USB3.0 Port1 (IO Board)

Layout Note: Need to Close CON

5V_S5
C3535 SCD1U16V2KX-3DLGP
USB_PWR_EN#
U3503
IN OUT GND EN# OC#
SY6288DAAC-GP
074.06288.009B
2nd = 074.00524.0C9F
USB_OC0#

USB30_VCCA
C3516 SCD1U16V2KX-3DLGP
C3517 SC1U10V2KX-1DLGP
C3515 SC220U6D3VM3X-1DLGP
C3514 SC220U6D3VM3X-1DLGP
DY

USB1_USB31_RX_N
USB1_USB31_RX_CON_N
EL3508
DLW21SN900SQ2LUGP
68.00201.031
2ND = 69.10171.001
USB1_USB31_RX_P
USB1_USB31_RX_CON_P

USB1_USB31_TX_N
C3534 SCD1U16V2KX-3DLGP
USB1_USB31_TX_CMC_N
USB1_USB31_TX_CON_N
EL3506
DLW21SN900SQ2LUGP
68.00201.031
2ND = 69.10171.001
USB1_USB31_TX_P
C3522 SCD1U16V2KX-3DLGP
USB1_USB31_TX_CMC_P
USB1_USB31_TX_CON_P

USB1_USB20_N
USB1_USB20_CON_N
EL3507
DLM0NSN900HY2D-GP
068.09002.2001
2nd = 68.02002.061
USB1_USB20_P
USB1_USB20_CON_P

ED3509
AZ1043-04F-R7G-GP
075.01043.0073
2nd = 075.08810.0A73
USB1_USB31_RX_CON_N
USB1_USB31_RX_CON_P
USB1_USB31_TX_CON_N
USB1_USB31_TX_CON_P

ED3508
AZ5315-02F-GP
83.05315.0A0
2nd = 075.5V0X2.0070
USB1_USB20_CON_N
USB1_USB20_CON_P

USB30_VCCA
USB2
VBUS
D-
D+
SSRX-
SSRX+
SSTX-
SSTX+
GND
PGND
CHASSIS#10
CHASSIS#11
CHASSIS#12
CHASSIS#13
USB1_USB20_CON_N
USB1_USB20_CON_P
USB1_USB31_RX_CON_N
USB1_USB31_RX_CON_P
USB1_USB31_TX_CON_N
USB1_USB31_TX_CON_P
SKT-USB13-442-GP-U
022.10005.0GK1
2ND = 022.10005.0GB1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.1 Gen1 Port1

Size	Document Number	Rev
A2	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 35 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB30

Size	Document Number	Rev
A4	***NAKIA_SHURI_N7_TGL-U***	***A00***

Date: Wednesday, August 05, 2020 Sheet 36 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	***NAKIA_SHURI_N7_TGL-U***	***A00***

Date: Wednesday, August 05, 2020 Sheet 37 of 106

Main Func = USB3.0 Redriver

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB30

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 38 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	***NAKIA_SHURI_N7_TGL-U***	***A00***

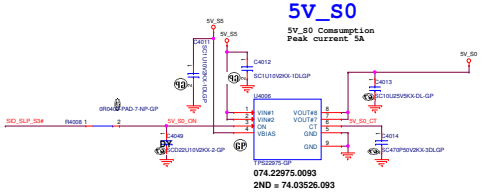
Date: Wednesday, August 05, 2020 Sheet 39 of 106

SSID = Power Plane & Sequence

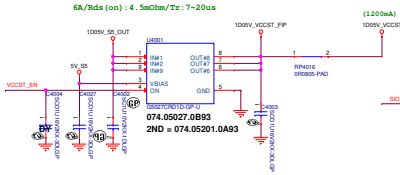
RUN Power

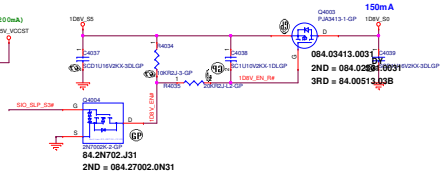
5V_S0

5V_S0 Comsumption
Peak current 5A



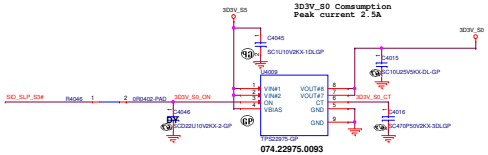
6A/Rds(on):4.5mOhm/Tr:7~20us



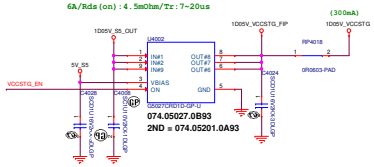


3D3V_S0

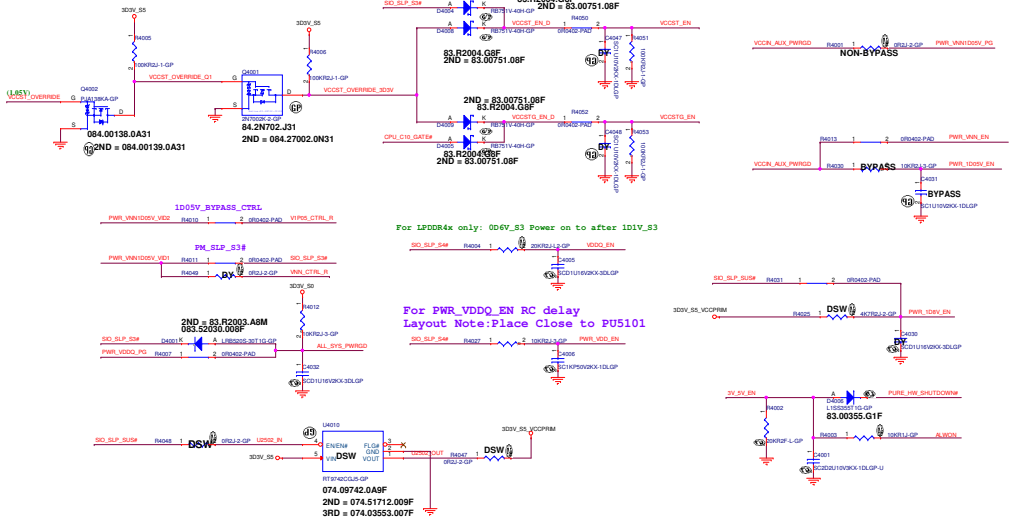
3D3V_S0 Comsumption
Peak current 2.5A



6A/Rds(on):4.5mOhm/Tr:7~20us

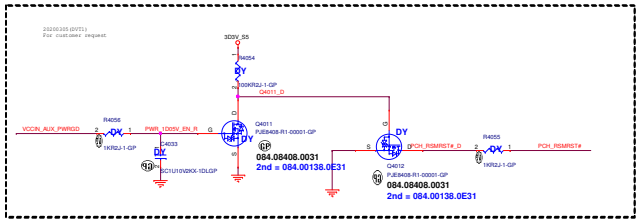


Power Sequence / Pull High PWRGD



For LPDDR4x only: 0D6V_S3 Power on to after 1D1V_S3

For PWR_VDDQ_EN RC delay
Layout Note:Place Close to PU5101



(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Connected_Standby(1/2)+DS3

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 41 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Connected_Standby(2/2)*

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 42 of 106

Main Func = ADT Input

[24] PS_ID
[24,44] AC_DIS
[24,44] HW_ACAVIN_NB
[24,44] PBAT_PRES#
[24,44] PBAT_CHG_SMBCLK
[24,44] PBAT_CHG_SMBDAT

+DC_IN_C
SC1K250V2KX-1DLGP
JGND

Layout Note:
PSID Layout width > 25mil

R4302 15KR2F-GP
PQ3802_1
Q4302 LMBT3904LT1G-GP
84.T3904.H11
2ND = 084.03904.0I11
3RD = 084.03904.0H11
R4309 100KR2J-1-GP
Q4301 PJA138KA-GP
PSID_DISABLE#_R_C
R4303 10KR2J-3-GP
5V_S5
3D3V_S5
D4302 LBAV99LT1G-1-GP
75.00099.O7D
2ND = 75.00099.E7D
3RD = 75.00099.B7D
R4304 2K2R2J-2-GP
PS_ID
PS_ID_R
R4317 0R0603-PAD
PS_ID_R2
PS_ID_R1
R4305 33R2J-2-GP
084.00138.0A31
D4303 AZ5125-02S-R7G-GP
2ND = 084.00139.0A31
75.05125.07D
2ND = 075.52215.007D

DCIN1
ACES-CON6-GP-U2
20.F1295.008
2ND = 20.F2120.008
EL4304 0R0805-PAD
EL4303 0R0805-PAD
AFTP4301
AFTP4302
60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA
D4301 P6AF24A-R1-00001-GP
083.00624.00AM
2ND = 083.FJ24A.00AM
EL4301 0R0805-PAD
EL4302 0R0805-PAD
C4302 SCD1U25V2KX-1DL-GP
C4301 SC10U25V5KX-DL-GP
C4307 SC1U25V5KX-1DLGP
19V_AD_JK
R4307 240KR3-GP
R4308 47KR2F-GP
PU4301 AONR21357-GP
084.21321.0037
2ND = 084.03307.0037
19V_AD+
C4306 SC10U25V5KX-DL-GP
C4303 SCD01U25V2KX-3DLGP
R4316 20KR2J-L2-GP

S1

AFTP4304
AFTP4303
AFTP4305
AFTP4316
AC_DIS
R4310 100KR2J-1-GP
Q4304 LMUN5212T1G-GP
84.05212.B11
2ND = 84.00124.H1K
3RD = 084.00024.0B1K
Q4305 LMUN5112T1G-GP-U
084.05112.001K
2ND = 84.00124.K1K
3RD = 084.00024.0A1K
AD_OFF_L
AD_OFF_R

Main Func = M-BAT Input

Batt Connecter

PBAT_PRES1#
KBC_SMB_SDA_BAT
KBC_SMB_SCL_BAT
BT+
AFTP4309
AFTP4310
AFTP4311
AFTP4312
AFTP4313
AFTP4314
SCD22U25V3KX-DL-GP
SC1K250V2KX-1DLGP
D4304 SMF18A-GP
BATT1
ACES-CON12-12-GP-U1
20.F0818.012
2ND = 020.F0243.0012
PBAT_CHG_SMBCLK
PBAT_CHG_SMBDAT
RN4302 SRN100J-3-GP
KBC_SMB_SCL_BAT
KBC_SMB_SDA_BAT
PBAT_PRES1#
PBAT_PRES#
R4327 100R2J-2-GP
AFTP4306
AFTP4307
AFTP4308
SC10P50V2JN-4DLGP

Barrel Adapter Piug-in Detect

3D3V_S5
R4313 200KR2F-L-GP
R4320 100KR2F-L1-GP
C4308 SC10P50V2JN-3DLGP
19V_AD_JK
R4328 150KR2F-L-GP
R4319 15KR2F-GP
C4307 SC10P50V2JN-3DLGP
U4302 AS331KTR-G1-GP
INPUT-
GND
INPUT+
VCC
OUTPUT
U4301-
U4301+
R4378 100KR2J-1-GP
HW_ACAVIN_NB
74.00331.H2F
2ND = 74.00391.02F

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
DCIN		
Size A3	Document Number NAKIA_SHURI_N7_TGL-U	Rev A00
Date: Wednesday, August 05, 2020	Sheet 43 of 106	

Main Func = Charger

ISL9538C For Charger

OFFPAGE

EE needs check it!!

- [24,43] PBAT_CHG_SMBDAT
- [24,43] PBAT_CHG_SMBCLK
- [24,64] HW_ACAV_IN
- [17] AC_INT
- [24,78] GPU_PWR_LEVEL
- [24] AD_IA
- [24,43] PBAT_PRES#
- [72] VCCPD_VBUS_ACK — From MXP ACK
- [24,43] AC_DIS
- [24,43] HW_ACAVIN_NB
- [3,22,24,44] PROCHOT#_CPU
- [64] PWR_CHG_CSOP_R
- [64] PWR_CHG_CSON_R
- [46] PWR_CORE_PSYS
- [17,24,40,46] ALL_SYS_PWRGD
- [46] PWR_VCORE_VR_READY

S2

PU +VCCSTG = 1.0 V on CPU side

Barrel Prochot — Follow custormer circuits.

TypeC Prochot — Follow custormer circuits.

10.85*10^3 DCR=8~9mohm Idc=13A, Isat=16A

+3D3V_VDD_DCIN

TypeC input / Barrel input

20V>+DC_IN>4.7V

Vout=1.24*(1+(R1/R2))

Vcore_OVP

CPU_Core / Charger LDO

ALL DY

Location	Gen11	Gen10
PR44A0	DY	Stuff
PR44D6	DY	Stuff
PR44D7	DY	Stuff
PR44D8	DY	Stuff
PC44D0	Stuff	DY
PC44D1	Stuff	DY
PQ44D1	Stuff	DY
PR44D0	Stuff	DY
PR44D1	Stuff	DY
PR44D2	Stuff	DY
PR44D3	Stuff	DY
PR44D4	Stuff	DY
PR44D5	Stuff	DY
PR44A7	Stuff	Stuff
PR44A8	DY	DY
PC44D0	Stuff	Stuff

Default:Gen11

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

INTEL CONFIDENTIAL
DEVELOPMENT

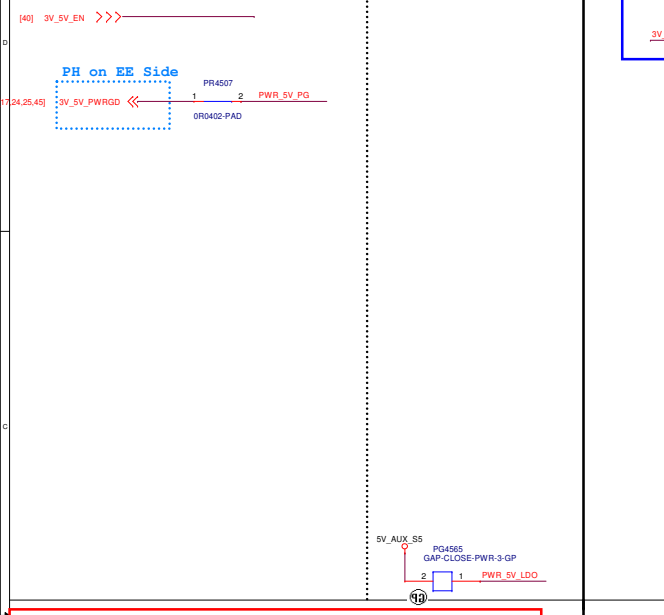
Wistron Corporation
Power (Charger_ISL9538)
NAKIA_SHURI_N7_TGL-U
A00

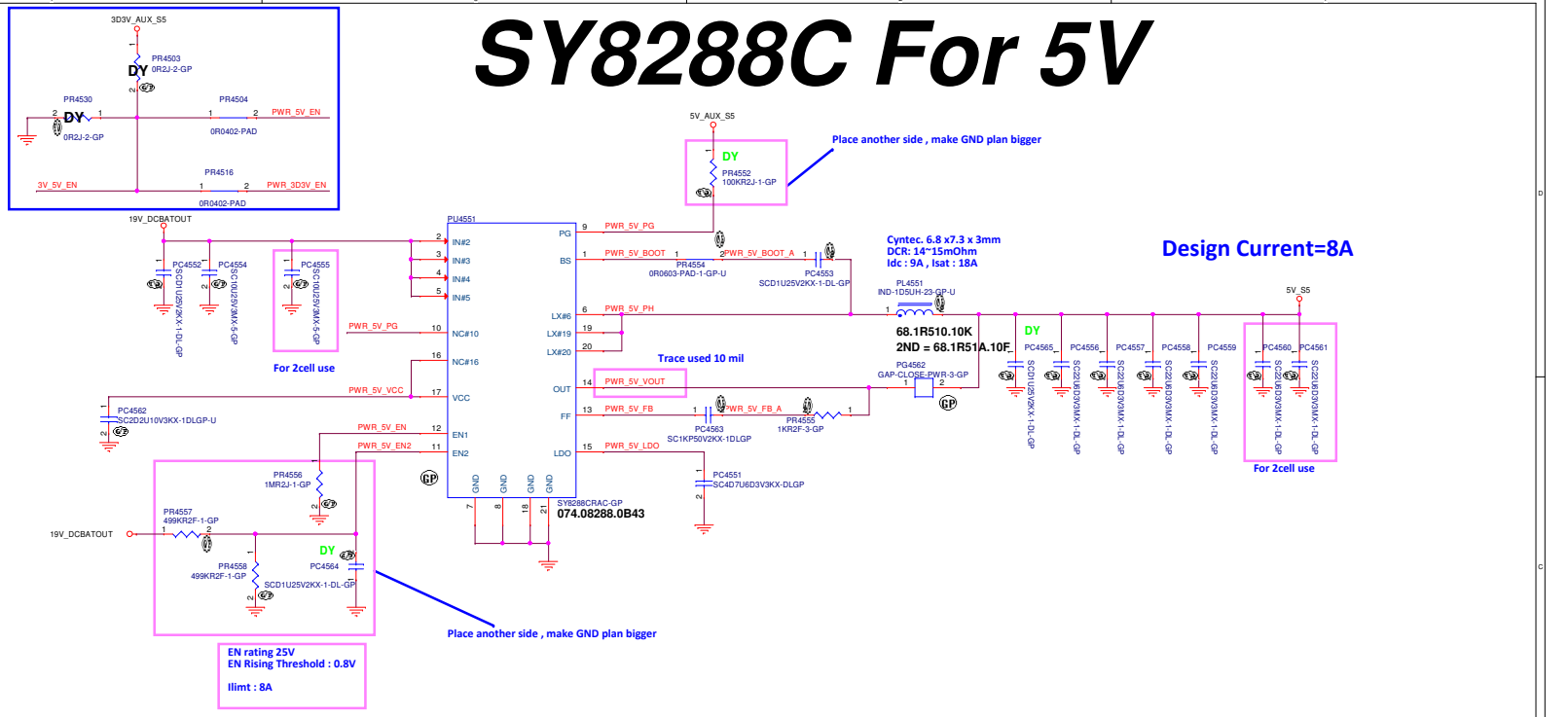
SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal

OFFPAGE-GAP

SY8288C For 5V



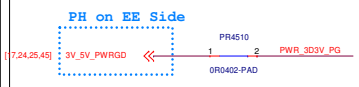


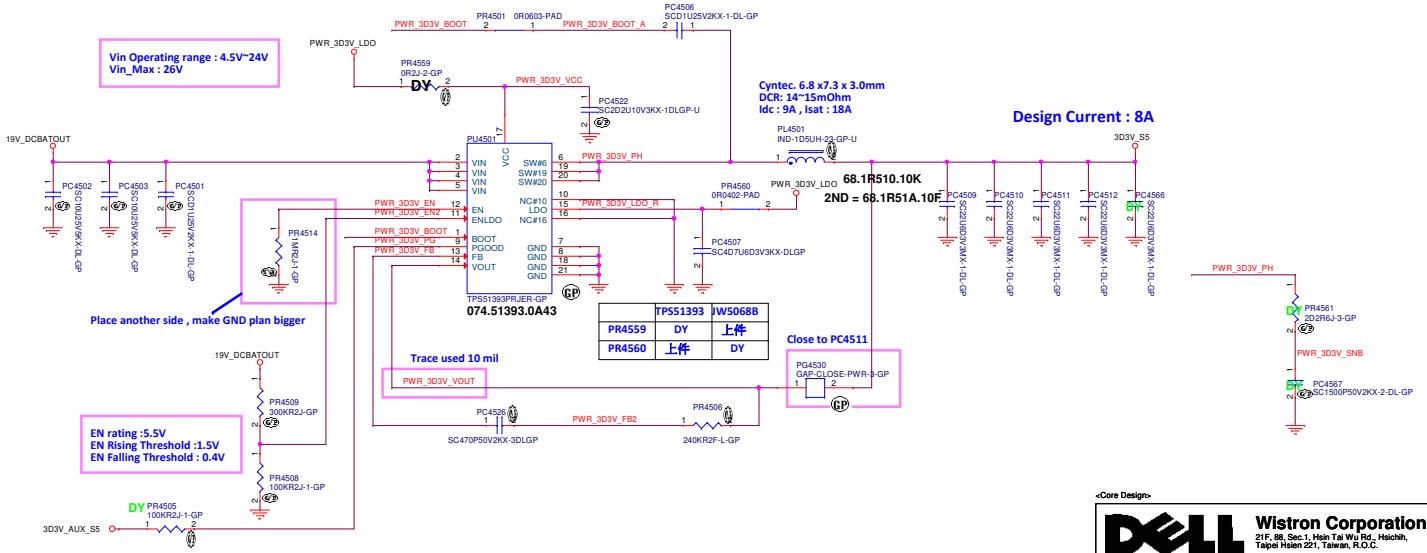
SSID = PWR.Plane.Regulator_3D3V

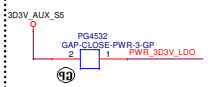
OFFPAGE-Signal

OFFPAGE-GAP

TPS51393 For 3D3V







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (SY8288_5V/3D3V)

Size: A2 | Document Number: STD | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 45 of 106

Main Func = CPU_CORE

OFFPAGE

SVID

- [7] SVID_CLK_CPU — PR4632 0R0402-PAD-1-GP — PWR_VCORE_SCLK_R
- [7] SVID_DATA_CPU — PR4633 0R0402-PAD-1-GP — PWR_VCORE_SDIO_R
- [7] SVID_ALERT#_CPU — PR4634 0R0402-PAD-1-GP — PWR_VCORE_ALERT#_R

- [3,22,24,44] PROCHOT#_CPU — PR4631 0R0402-PAD-1-GP — PWR_VCORE_VRHOT_R
- [44] PWR_CORE_PSYS — PWR_CORE_PSYS
- [44] PWR_VCORE_VR_READY — PR4636 0R0402-PAD-1-GP — PWR_VCORE_VR_READY
- [3,40,44] ALL_SYS_PWRGD — PR4635 0R0402-PAD-1-GP — PWR_VCORE_VR_EN

VCORE SENSE

- [7] VSSCORE_SENSE — VSSCORE_SENSE
- [7] VCCCORE_SENSE — VCCCORE_SENSE

- [47] PWR_VCORE_UGATE1 — PWR_VCORE_UGATE1
- [47] PWR_VCORE_PHASE1 — PWR_VCORE_PHASE1
- [47] PWR_VCORE_LGATE1 — PWR_VCORE_LGATE1

- [47] PWR_VCORE_UGATE2 — PWR_VCORE_UGATE2
- [47] PWR_VCORE_PHASE2 — PWR_VCORE_PHASE2
- [47] PWR_VCORE_LGATE2 — PWR_VCORE_LGATE2

- [47] PWR_VCORE_ISEN2 — PWR_VCORE_ISEN2
- [47] PWR_VCORE_ISEN1 — PWR_VCORE_ISEN1
- [47] PWR_VCORE_ISUMP — PWR_VCORE_ISUMP
- [47] PWR_VCORE_ISUMN — PWR_VCORE_ISUMN

	U22	U42
PR4620	13.3K(64.13325.6DL)	9.31K(64.93115.6DL)
PR4608	76.8K(64.76825.6DL)	88.7K(64.88725.6DL)
PR4615	1.3K(64.13015.6DL)	1.3K(64.13015.6DL)
PR4613	1.27K(64.12715.6DL)	2.87K(64.28715.6DL)
PR4627	365(64.36505.6DL)	511(64.51105.6DL)
PR4610	0(64.R0005.6DL)	DY
PC4614	DY	0.022u(78.22321.2FLDL)
PC4618	DY	0.022u(78.22321.2FLDL)
PC4616	0.047u(78.47321.2FLDL)	0.022u(78.22321.2FLDL)
PC4602	0.033u(78.33321.2FLDL)	0.1u(78.10421.2FLDL)

1D05V_VCCST — PC4639 SCD1U25V2KX-1-DL-GP

PR4606 100KR2F-L-GP-U — PR4621 100KR2F-L-GP-U — PR4622 100KR2F-L-GP-U — PR4623 100KR2F-L-GP-U — PR4624 100KR2F-L-GP-U

PWR_VCORE_SCLK_R
PWR_VCORE_ALERT#_R
PWR_VCORE_SDIO_R

1D05V_VCCST — PR4603 1KR2F-3-GP (DY)

PWR_VCORE_VRHOT_R — PR4607 100R2F-L1-GP-U

3D3V_S0 — PR4609 10KR2F-2-GP

5V_S5 — PR4617 0R0402-PAD — PC4613 SC1U10V2KX-1DLGP

PR4601 0R0402-PAD — 19V_DCBATOUT — PC4601 SCD22U25V2KX-4-GP

PWR_VCORE_VR_EN

PC4612 SC4700P50V2KX-1DLGP — PR4602 12K1R2F-L1-GP (DY)

PC4609 SC330P50V2KX-3-DL-GP — PR4608 88K7R2F-GP

U42=64.88725.6DL,U22=64.76825.6DL

PU4601 ISL95869HRTZ-T-GP 074.95869.0073

PWR_CORE_PSYS — PSYS
PWR_VCORE_IMON — IMON
PWR_VCORE_NTC — NTC
PWR_VCORE_COMP — COMP
PWR_VCORE_FB — FB
PWR_VCORE_RTN — RTN
PWR_VCORE_ISUMN — ISUMN
ISUMP

GND, VR_ENABLE, VR_READY, SCK, SDIO, ALERT#, SVID, VDD, VIN

PWR_VCORE_VR_READY, PWR_VCORE_VRHOT, PWR_VCORE_ALERT#, PWR_VCORE_SDIO, PWR_VCORE_SCK, PWR_VCORE_VIN

PROG1 — PWR_VCORE_PROG1
PROG2 — PWR_VCORE_PROG2
BOOT1 — PWR_VCORE_BOOT1
UGATE1 — PWR_VCORE_UGATE1
PHASE1 — PWR_VCORE_PHASE1
LGATE1 — PWR_VCORE_LGATE1
PWM3
VDDP — PWR_VCORE_VDDP

ISL95869
ICL-U PROG1=9.31K to GND, VBOOT=1.8V.
TGL-U PROG1=78.7K to GND, VBOOT=0V.

PR4619 78K7R2F-GP — PR4620 9K31R2F-GP (U42=64.93115.6DL,U22=64.13325.6DL)

PR4621 0R0603-PAD — PWR_VCORE_BOOT1_N — PC4610 SCD22U25V2KX-4-GP

PR4625 0R0402-PAD — O5V_S5 — PC4625 SC1U10V2KX-1DLGP

PR4611 0R0603-PAD — PWR_VCORE_BOOT2_N — PC4611 SCD22U25V2KX-4-GP — O5V_S5

PWR_VCORE_BOOT2, PWR_VCORE_UGATE2, PWR_VCORE_PHASE2, PWR_VCORE_LGATE2

USEN1, USEN2, ISEN1, ISEN2, FCCM, BOOT2, UGATE2, PHASE2, LGATE2

PR4616 10KR2F-2-GP — PWR_VCORE_NTC_N — PR4618 B=4500 NTC-47K-17-GP 069.60012.0001 (2nd ~ 069.60006.0001) — PR4655 27K4R2F-GP

PR4615 1K3R2F-1-GP — PC4608 SC82P50V2JN-3-DL-GP

PWR_VCORE_COMP_N — PC4607 SC1U10V2KX-3DLGP

PR4614 2KR2F-3-GP (DY) — PR4613 24K9R2F-1-GP (U42=64.28715.6DL,U22=64.12715.6DL) — PR4612 392R2F-GP

PWR_VCORE_FB1 — PC4606 SC330P50V2KX-3-DL-GP (DY)

PWR_VCORE_FB2 — PC4604 SC820P50V2KX-1-DL-GP

PWR_VCORE_FB4

VCCCORE_SENSE — PR4667 0R0402-PAD-1-GP — PR4640 100R2F-L1-GP-U — VCCIN

PWR_VCORE_FB3 — PR4665 0R0402-PAD — PC4615 SCD01U25V2KX-3DLGP (DY)

PR4666 0R0402-PAD-1-GP — VSSCORE_SENSE

PC4605 SC330P50V2KX-3-DL-GP — PC4638 SC330P50V2KX-DL-GP — PR4626 100R2F-L1-GP-U

PC4623 SC2200P50V2KX-2DLGP — PWR_VCORE_ISUMN_N — PR4628 3K48R2F-GP

PR4627 511R2F-2-GP (U42=64.51105.6DL,U22=64.36505.6DL)

PWR_VCORE_ISEN2
PWR_VCORE_ISEN1
PWR_VCORE_ISUMP

PR4629 0R0402-PAD — PWR_VCORE_ISUMP_N — PC4616 SCD22U25V2KX-3DLGP

PC4614 SCD22U25V2KX-3DLGP — PC4618 SCD22U25V2KX-3DLGP — PC4602 SCD1U16V2KX-3DLGP

PR4630 11KR2F-L-GP — PR4653 2K61R2F-1-GP — PWR_VCORE_ISUMNP_2 — PR4650 NTC-10K-29-GP-U B=3370 69.60011.201 (2nd ~ 69.60013.151) — PWR_VCORE_ISUMN

PC4603 SCD01U50V2KX-1DLGP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (95829_CPUCORE(2/3))

Size: A2 | Document Number: Vader15"/17" CML | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 46 of 106

Main Func = VCCIN

OFFPAGE

[46] PWR_VCORE_UGATE1 — PWR_VCORE_UGATE1
[46] PWR_VCORE_PHASE1 — PWR_VCORE_PHASE1
[46] PWR_VCORE_LGATE1 — PWR_VCORE_LGATE1

[46] PWR_VCORE_UGATE2 — PWR_VCORE_UGATE2
[46] PWR_VCORE_PHASE2 — PWR_VCORE_PHASE2
[46] PWR_VCORE_LGATE2 — PWR_VCORE_LGATE2

[46] PWR_VCORE_ISEN2 — PWR_VCORE_ISEN2
[46] PWR_VCORE_ISEN1 — PWR_VCORE_ISEN1
[46] PWR_VCORE_ISUMP — PWR_VCORE_ISUMP
[46] PWR_VCORE_ISUMN — PWR_VCORE_ISUMN

[66] DCBATOUT_VCOREA_P — DCBATOUT_VCOREA_P
[66] DCBATOUT_VCOREA_N — DCBATOUT_VCOREA_N

19V_DCBATOUT
PWR_DCBATOUT_VCOREA
RP4701 D01R5F-GP
RP4702 D01R5F-GP
R4701 DY 0R1J-GP
R4702 DY 0R1J-GP
DCBATOUT_VCOREA_P
DCBATOUT_VCOREA_N

PD4701 1st = B3 PJS1220AF 2nd = 083.0062.0AA1
PC4717 SC101U25V3MX-5-GP
PC4714 SC101U25V3MX-5-GP
PC4716 SC101U25V3MX-5-GP
PC4715 SC101U25V3MX-5-GP
PC4718 SC2D1U25V2KX-1-DL-GP
PT4702 ST100U25VDM-1-GP

PWR_VCORE_LGATE1
PWR_VCORE_UGATE1
PWR_VCORE_PHASE1
PWR_DCBATOUT_VCOREA
PU4701 AOE6932-GP
075.06932.0A73
2ND = 075.24038.0073

TGL_U42 28W
Performance
TDC=38A
ICCMAX=62A

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

VCCIN
PL4701 IND-D15UH-33-GP
068.R1510.1171
2nd = 068.R1510.1141
PT4701 SE330U2D5VDM-2GP
79.3371V.2PL
2ND = 80.3371V.L01
PR4705 2D2R6J-3-GP
PG4711 GAP-CLOSE-PWR-3-GP
PG4712 GAP-CLOSE-PWR-3-GP
PWR_VCORE_SNB1
PC4710 SC1KP50V2KX-1DLGP
PWR_VCORE_ISUMP_GA
PWR_VCORE_ISUMN_GA
PR4721 100KR2F-L1-GP
PR4709 10R2F-L-GP
PR4722 100KR2F-L1-GP
PR4708 3K65R2F-1-GP
PWR_VCORE_ISEN1
PWR_VCORE_ISUMP
PWR_VCORE_ISUMN
PWR_VCORE_ISEN2

PWR_DCBATOUT_VCOREA
PC4702 PC4703 PC4704 PC4705 PC4706 SC101U25V3MX-5-GP
SC2D1U25V2KX-1-DL-GP

PWR_VCORE_LGATE2
PWR_VCORE_UGATE2
PWR_VCORE_PHASE2
PWR_DCBATOUT_VCOREA
PU4702 AOE6932-GP
075.06932.0A73
2ND = 075.24038.0073

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

VCCIN
PL4702 IND-D15UH-33-GP
068.R1510.1171
PR4714 2D2R6J-3-GP
PG4713 GAP-CLOSE-PWR-3-GP
PG4714 GAP-CLOSE-PWR-3-GP
PWR_VCORE_SNB2
PC4713 SC1KP50V2KX-1DLGP
PWR_VCORE_ISUMP_GB
PWR_VCORE_ISUMN_GB
PR4723 100KR2F-L1-GP
PR4716 3K65R2F-1-GP
PR4715 0R2F-L-GP
PR4724 100KR2F-L1-GP
PWR_VCORE_ISEN2
PWR_VCORE_ISUMP
PWR_VCORE_ISUMN
PWR_VCORE_ISEN1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT6543A_VCCIN_AUX
Size: A2
Document Number:
Rev: A00
Date: Wednesday, August 05, 2020
Sheet 47 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Size: A3	Document Number	Rev: A00
Date: Wednesday, August 05, 2020	Sheet 48 of 105	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER (RSVD)***

Size	Document Number	Rev
A	***NAKIA_SHURI_N7_TGL-U***	***A00***

Date: Wednesday, August 05, 2020 Sheet 49 of 106

Main Func = VCCIN_AUX

OFFPAGE

VID

PR5014 0R0402-PAD-7-NP-GP
[22] CORE_VID0 — PWR_VCCIN_AUX_VID0
PR5015 0R0402-PAD-7-NP-GP
[22] CORE_VID1 — PWR_VCCIN_AUX_VID1

PR5012 0R0402-PAD
[24,53] PWR_1D8V_PG — PWR_VCCIN_AUX_EN_R
PR5013 0R0201-PAD-2-GP
[17,24,40] VCCIN_AUX_PWRGD — PWR_VCCIN_AUX_PG

VCCIN_AUX SENSE

PR5017 0R0402-PAD-7-NP-GP
[22] VCCAUX_SENSE — PWR_VCCIN_AUX_FB_O
PR5018 0R0402-PAD-7-NP-GP
[22] VSSAUX_SENSE — PWR_VCCIN_AUX_RGND

[66] VCCIN_AUX_P
[66] VCCIN_AUX_N

19V_DCBATOUT
PWR_VCCIN_AUX_IN
RP5001 0R1R5E-4P
RP5002 0R1R5E-4P
R5001 0R1J-GP
R5002 0R1J-GP
VCCIN_AUX_P
VCCIN_AUX_N

PWR_VCCIN_AUX_IN
FC5017 SC1P2N2V2KX-DLGP
FC5018 SC2P2P50V2KN-DLGP
PC5006 SC10U6V3MX-5GP
PC5007 SC10U6V3MX-5GP
PC8638 SC10U6V3MX-5GP
PC8639 SC10U6V3MX-5GP

PWR_VCCIN_AUX_LX
FC5019 SC1P2N2V2KX-DLGP

PC5009 SC1U10V2KX-1DLGP
PWR_VCCIN_AUX_BOOT

PU5001 RT6543AGQW-GP
074.06543.0073

Pin	Name	Net
1	CS_DIS	PWR_VCCIN_AUX_CS
15	PVCC	PWR_VCCIN_AUX_VCC
16	VCC	
4	PG	PWR_VCCIN_AUX_PG
19	EN	PWR_VCCIN_AUX_EN
17	VID1	PWR_VCCIN_AUX_VID1
18	VID0	PWR_VCCIN_AUX_VID0
9	FSWSEL	PWR_VCCIN_AUX_FSW
21	AGND	
10	BOOT	PWR_VCCIN_AUX_BOOT
20	VSYS	PWR_VCCIN_AUX_IN
11	UG	PWR_VCCIN_AUX_UG
12	PH	PWR_VCCIN_AUX_LX
13	LG	PWR_VCCIN_AUX_LG
14	PGND	
2	ISENSEP	PWR_VCCIN_AUX_ISENP
3	ISENSEN	PWR_VCCIN_AUX_ISENN
8	VOUT	1D8V_VCCIN_AUX
5	COMP	PWR_VCCIN_AUX_COMP
6	FB	PWR_VCCIN_AUX_FB
7	RGND	PWR_VCCIN_AUX_RGND

PR5002 124KR2F-GP
PR5001 2D2R2J-GP
PR5004 10KR2F-2-GP
PC5008 SC1U10V2KX-1DLGP
PR5005 2D2R2J-GP
PC5010 SC1U10V2KX-1DLGP
PR5003 10KR2F-2-GP
3D3V_S5
5V_S5

PWR_VCCIN_AUX_IN
PU5002 AON6994-GP
075.06994.0037
075.07321.0073
075.36354.0073
PU5003 AON6994-GP
075.06994.0037
075.07321.0073
075.36354.0073

TGL_U42 28W
Performance
TDC=16A
ICCMAX=32A

Cyntec. 6.8 x 7.3 x 3mm
DCR: 2.5~2.8 mOhm
Idc : 23A , Isat : 40A

PL5001 IND-D22UH-37-GP
68.R2210.10V
2nd = 068.R2210.1521
PG5001 GAP-CLOSE-PWR-3-GP
PG5002 GAP-CLOSE-PWR-3-GP
PT5001 SE330U2D5VDM-2GP
1D8V_VCCIN_AUX

PWR_VCCIN_AUX_ISENP_A
PWR_VCCIN_AUX_ISENN_A
PR5021 5K36R2F-GP
PR5016 0R0402-PAD
PR5007 100R2F-L1-GP-U
PC5011 SCD1U25V2KX-1-DL-GP
PR5008 267R2F-1-GP
PR5022 866R2F-GP
PWR_VCCIN_AUX_RC
3/19 For LL 3.3m ohm
PR5023 NTC-10K-29-GP-U
B=3370K
PWR_VCCIN_AUX_FB_O

PC5003 SC2200P50V2KX-2DLGP
PWR_VCCIN_AUX_COMP_R
PR5011 10KR2F-2-GP
PC5002 SC470P50V2KX-3DLGP
PWR_VCCIN_AUX_FB_R
PR5009 1K6R2F-GP
PC5004 SC22P50V2JN-4DLGP
PR5010 5K62R2F-GP
PR5006 100R2F-L1-GP-U
PR5020 0R0402-PAD

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT6543A_VCCIN_AUX
Size: A2 | Document Number | Rev: A00
Date: Wednesday, August 05, 2020 | Sheet 50 of 106

SSID = PWR.Plane.Regulator_1.1V/0.6V

S5(PM_SLP_S4#)

[40] PWR_VDD_EN → PWR_VDD_EN

S3(VTT_CNTL)

[40] VDDQ_EN → VDDQ_EN

PH on EE Side

[40] PWR_VDDQ_PG → PWR_VDDQ_PG

[66] DCBATOUT_VDDQ_P

[66] DCBATOUT_VDDQ_N

OFFPAGE_GAP

19V_DCBATOUT, PWR_DCBATOUT_VDDQ

PG5101 GAP-CLOSE-PWR-3-GP

PG5102 GAP-CLOSE-PWR-3-GP

R5101 DY 0R1J-GP

R5102 DY 0R1J-GP

DCBATOUT_VDDQ_P

DCBATOUT_VDDQ_N

1D1V_S3, PWR_VDDQ

PG5131 GAP-CLOSE-PWR-3-GP

PG5132 GAP-CLOSE-PWR-3-GP

PG5121 GAP-CLOSE-PWR-3-GP

PG5120 GAP-CLOSE-PWR-3-GP

PG5125 GAP-CLOSE-PWR-3-GP

PG5122 GAP-CLOSE-PWR-3-GP

PG5129 GAP-CLOSE-PWR-3-GP

PG5130 GAP-CLOSE-PWR-3-GP

1D1V_S3, PWR_VDDQ_VLDOIN

RP5124 0R0603-PAD

0D6V_VREF_S0, PWR_VDDQ_VTT

RP5122 0R0805-PAD

1P8V_S3, PWR_VDDQ_1D8V

PG5126 GAP-CLOSE-PWR-3-GP

PWR_DCBATOUT_VDDQ

PC5101 SC10U25V5KX-DL-GP

PC5102 SC10U25V5KX-DL-GP

PC5117 SCD1U25V2KX-1-DL-GP

PC5103 SC10U6D3V3MX-DL-GP

5V_S5, PR5110 0R0402-PAD-1-GP

PR5107 0R0402-PAD-1-GP

PC5113 SC1U10V2KX-1DLGP

3D3V_S5, PR5108 100KR2F-L1-GP

PC5104 SC10U6D3V3MX-DL-GP

PC5116 SCD1U16V2KX-3DLGP

PR5101 0R0402-PAD

VDDQ_EN

PU5101 TPS51487XRJER-1-GP

074.51487.M002

PWR_VDDQ_VCC, PWR_VDDQ_VDD1, PWR_VDDQ_PG, PWR_VDD_EN, PWR_VDDQ_EN, PWR_VDDQ_VLDOIN

PWR_VDDQ_BOOT_A

PR5109 5D1R3F-GP

PC5108 SCD1U25V2KX-1-DL-GP

PWR_VDDQ_BOOT

PL5102 COIL-D68UH-9-GP

Cyntec. 6.6mmx7.3mmx3.0 mm
DCR:4.8~5.3mOhm
Idc :16A , Isat : 17A

68.R6810.20J
2ND = 68.R681A.10A

VDDQ:Design Current=8A

PWR_VDDQ

PC5109 PC5110 PC5111 PC5112 PC5115 SC22U6D3V3MX-1-DL-GP

PR5106 DY 2D2R6J-3-GP

PWR_VDDQ_SNB

PC5114 DY SC1500P50V2KX-2-DL-GP

PG5133 GAP-CLOSE-PWR-3-GP

PWR_VDDQ_PH, PWR_VDDQ_SENSE, PWR_VDDQVTT_SENSE, PWR_VDDQ_VDDQREF, PWR_VDDQVTD8V_SENSE

PWR_VDDQ_VTT

VTT:Design Current=0.73A

PC5107 SC10U6D3V3MX-DL-GP

PR5104 0R0402-PAD

PC5106 SC1U10V2KX-1DLGP

PWR_VDDQ_1D8V

VDDQ:Design Current=0.2A

PL5101 IND-4D7UH-352-GP

068.4R710.1111
2ND = 068.4R710.1311

PC5105 SC22U6D3V3MX-1-DL-GP

PR5103 0R0402-PAD-1-GP

TOKO. 2.5mm×2.0mmX1.2mm
DCR: 240m Ohm
Idc : 1.3A , Isat :1.5A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 051_POWER (TPS51487X_VDDQ)

Size: Custom | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 51 of 106

Main Func = VCCST

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power (RT5797_VCCST)*

Size	Document Number	Rev
B	*NAKIA_SHURI_N7_TGL-U*	*A00*

Date: Wednesday, August 05, 2020 Sheet 52 of 106

Main Func = 1D8V/1D2V

OFFPAGE

PH on EE Side

[4,50] PWR_1D8V_PG <<< PWR_1D8V_PG

[40] PWR_1D8V_EN >>> PWR_1D8V_EN

EE confirm

[24] PRIM_PWRGD <<< PRIM_PWRGD

[17,40,55] SIO_SLP_S3# >>>

OFFPAGE_GAP

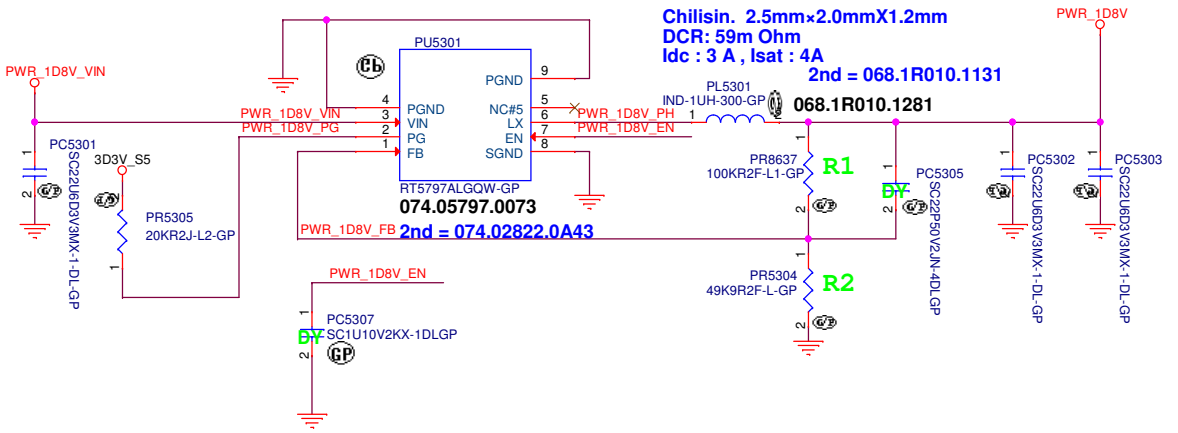
3D3V_S5 — RP5301 0R1R3F-2-GP — PWR_1D8V_VIN

1D8V_S5 — PG5303 GAP-CLOSE-PWR-3-GP — PG5304 GAP-CLOSE-PWR-3-GP — PG5305 GAP-CLOSE-PWR-3-GP — PWR_1D8V

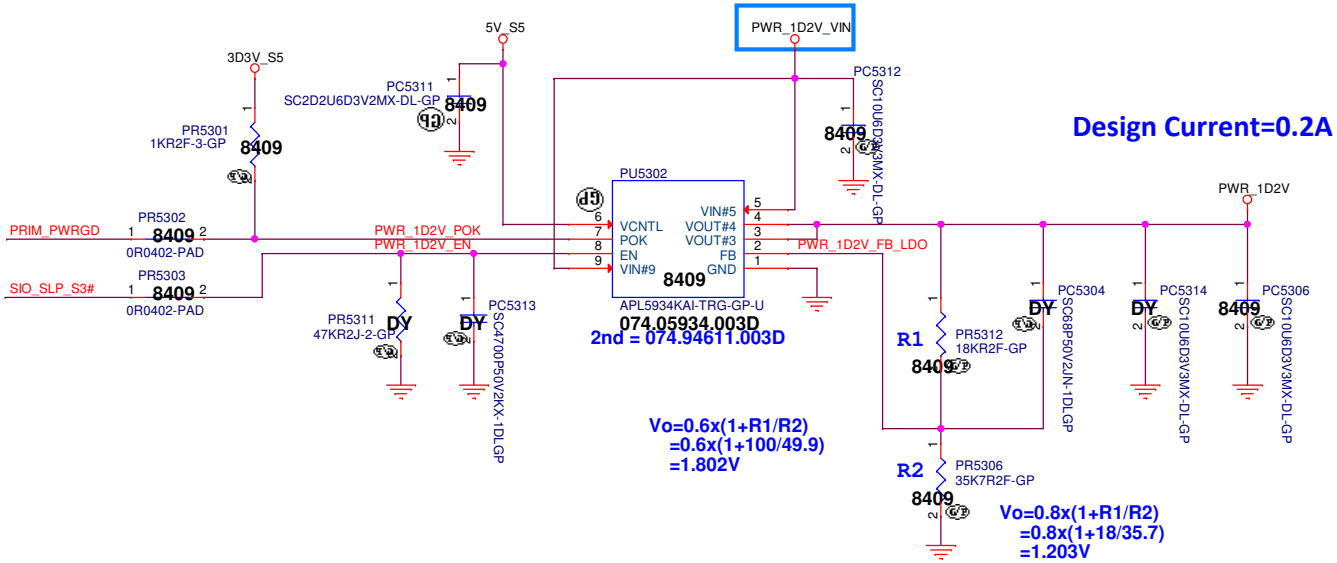
3D3V_S5 — RP5306 0R0603-PAD — PWR_1D2V_VIN

1D2V_HDMI — RP5307 0R0603-PAD — PWR_1D2V

Design Current=1.7A



Design Current=0.2A



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT6543A_VCCIN_AUX

Size: B | Document Number | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 53 of 106

SSID = PWR.Plane.Regulator_1.05V

PH on EE Side

VCCIN_AUX_PWRGD
[40] PWR_VNN_EN
PWR_VNN_EN

1D05V_BP_PWRGD
[40] PWR_VNN1D05V_PG
PWR_VNN1D05V_PG

[40] PWR_1D05V_EN
PWR_1D05V_EN

PH on EE Side

1D05V_BYPASS_CTRL
[40] PWR_VNN1D05V_VID2
PWR_VNN1D05V_VID2

PM_SLP_S3#
[40] PWR_VNN1D05V_VID1
PWR_VNN1D05V_VID1

VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

OFFPAGE-GAP

1D05V_VNN_BYPASS — RP5499 0R0603-PAD — PWR_VNN

1D05V_S5_BYPASS — RP5498 0R0603-PAD — PWR_1D05V

3D3V_S5 — PR5420 10KR2J-3-GP — PWR_VNN1D05V_PG

BYPASS

CHILISIN. 2.5mm×2.0mmX1.2mm
DCR: 59m Ohm
Idc : 3A , Isat : 4A

PL5401 IND-1UH-300-GP

PC5411 SC22U6D3V3MX-1-DL-GP

PC5412 SC22U6D3V3MX-1-DL-GP

Murata. 2.7mm×2.2mmX1.2mm
DCR: 460m Ohm
Idc : 0.85A , Isat : 1A

PL5402 IND-10UH-348-GP

068.10010.1341

2ND = 68.10015.10K

PC5414 SC100P50V2JN-3DLGP

PR5408 0R0402-PAD

PC5410 SC22U6D3V3MX-1-DL-GP

PC5413 SC22U6D3V3MX-1-DL-GP

PR5407 0R2J-2-GP

PR5419 0R0402-PAD-1-GP

PR5430 0R2J-2-GP

5V_S5 — PC5401 SC1U10V2KX-1DLGP — PR5413 0R0402-PAD

19V_DCBATOUT

PC5402 SC4D7U25V3KX-2-GP — PR5422 0R0402-PAD-1-GP — PR5410 0R0402-PAD-1-GP

PC5403 SC4D7U25V3KX-2-GP

PC5404 SCD1U25V2KX-1-DL-GP — PWR_VNN1D05V_BOOTA_A

PC5405 SCD1U25V2KX-1-DL-GP — PWR_VNN1D05V_BOOTB_A

PC5406 SCD1U16V2KX-3DLGP — PR5423 0R0402-PAD — PWR_VNN1D05V_PHB

PR5401 0R0402-PAD — PWR_VNN1D05V_PHA

PU5401 APW8743CQBI-TRG-GP

Pin	Signal
8	PWR_VNN1D05V_VCC
11	PWR_VNN1D05V_VINA
10	PWR_VNN1D05V_VINB
13	PWR_VNN1D05V_VID1
2	PWR_VNN1D05V_BOOTA
3	PWR_VNN1D05V_BOOTB
14	PWR_VNN1D05V_VID2
7	PWR_VNN1D05V_PG
15	PWR_VNN_EN
6	PWR_1D05V_EN
1	PWR_VNN1D05V_PHA
4	PWR_VNN1D05V_PHB
5	PWR_VNN1D05V_FB2
16	PWR_VNN1D05V_VOUT
17	AGND
9, 12	PGND

074.08743.0A73

3D3V_S5 3D3V_S5

PR5426 10KR2F-2-GP — PWR_VNN1D05V_VID1

PR5427 10KR2F-2-GP — PWR_VNN1D05V_VID2

PR5433 10KR2F-2-GP

PR5428 10KR2F-2-GP

VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APW8743_ByPASS

Size: Custom | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 54 of 106

Main Func = LCD

[4] eDP_TX_CPU_P0
[4] eDP_TX_CPU_N0
[4] eDP_TX_CPU_P1
[4] eDP_TX_CPU_N1
[4] eDP_TX_CPU_P2
[4] eDP_TX_CPU_N2
[4] eDP_TX_CPU_P3
[4] eDP_TX_CPU_N3
[4] eDP_AUX_CPU_P
[4] eDP_AUX_CPU_N
[4] EDP_HPD
[4] eDP_VDD_EN

[4] L_BKLT_CTRL
[24] LCD_TST
[24] PANEL_BKEN
[24] PANEL_MONITOR
[24] LCD_VCC_TEST_EN

[17,40,53] SIO_SLP_S3#
[24] CABLE1_OCP#
[24] CABLE2_OCP#
[16] CCD_USB20_P
[16] CCD_USB20_N
[27] DMIC_SCL_CODEC
[27] DMIC_SDA_CODEC
[19] DMIC_PCH_CLK
[19] DMIC_PCH_DATA

TGL
[20] DBC_PANEL_EN

[66] DCBATOUT_LCD_P
[66] DCBATOUT_LCD_N

[66] 3D3V_LCDVDD_P
[66] 3D3V_LCDVDD_N

CCD_USB20_N
CCD_USB20_P
EL5501
DLM0NSN900HY2D-GP
068.09002.2001
ED5501
AZ5315-02F-GP
83.05315.0A0
2nd = 075.5V0X2.0070

eDP_VDD_EN
LCD_VCC_TEST_EN
D5501
BAT54C-12-GP
75.00054.A7D
2ND = 75.00054.T7D
LVDS_VDD_EN
SIO_SLP_S3#
U5501
G2895ALK21U-GP
074.02895.0073
CABLE1_OCP#
CABLE2_OCP#
THERMAL_PAD

3D3V_S5
5V_S5
3D3V_LCDVDD_P
3D3V_LCDVDD_N
3D3V_LCDVDD_R
3D3V_LCDVDD_S0
R5543 0R1J-GP
R5544 0R1J-GP
RP5501 0R0805-PAD
C5502 SC4D7U6D3V2MX-1GP
C5543 SC4D7U6D3V2MX-1GP
C5542 SC1U25V2KX-1DLGP
C5508 SC1U10V2KX-1DLGP
C5507 SCD1U16V2KX-3DLGP

3D3V_HINGE_S0
C5516 SC1U16V3KX-3DLGP
RP5502 0R0402-PAD
RP5503 0R0402-PAD
3D3V_MIC_VCC
C5515 SC4D7U6D3V2MX-1GP
3D3V_CAMERA_S0
C5503 SC4D7U6D3V2MX-1GP

INVERTER POWER

19V_DCBATOUT
2ND = 69.50007.G71
69.50007.A21
F5503 POLYSW-1D1A24V-GP-U
R5541 0R1J-GP
R5542 0R1J-GP
19V_DCBATOUT_LCD
C5514 SC1U16V3KX-1DLGP
C5512 SC1U25V2KX-1DLGP
C5513 SC1KR56V2KX-1DLGP
DCBATOUT_LCD_P
DCBATOUT_LCD_N
CABLE1_OCP#
CABLE2_OCP#
R5504 0R0402-PAD-7-NP-GP

LCD_TST
PANEL_BKEN
RN5501 SRN100J-3-GP
LCD_TST_C
BLON_OUT_C
LCD_BRIGHTNESS
eDP_HPD_CON
RN5505 SRN100J-3-GP
BKLT_CTRL
eDP_RPD

R5502 0R2J-2-GP
D5502 BAT54C-12-GP
75.00054.A7D
2ND = 75.00054.T7D
L_BKLT_CTRL
LCD_TST
RN5502 SRN100KJ-5-GP
eDP_HPD_CON
LVDS_VDD_EN
BLON_OUT_C
BKLT_CTRL

3D3V_S5
RN5506 SRN10KJ-5-GP
RN5504 SRN33J-5-GP-U
RN5503 SRN33J-5-GP-U
DMIC_PCH_CLK
DMIC_PCH_DATA
DMIC_SCL_CODEC
DMIC_SDA_CODEC
DMIC_SCL_CON
DMIC_SDA_CON
EC5504 SC33P50V2JN-3DLGP
EC5503 SC33P50V2JN-3DLGP

eDP Panel / HD Camera

LCD1
19V_DCBATOUT_LCD
DBC_PANEL_EN
LCD_TST_C
eDP_HPD_CON
LCD_BRIGHTNESS
BLON_OUT_C
eDP_AUX_CPU_P C5510 SCD1U16V2KX-3DLGP eDP_AUX_CON_P
eDP_AUX_CPU_N C5511 SCD1U16V2KX-3DLGP eDP_AUX_CON_N
eDP_TX_CPU_P3 C5521 SCD1U16V2KX-3DLGP eDP_TX_CON_P3
eDP_TX_CPU_N3 C5522 SCD1U16V2KX-3DLGP eDP_TX_CON_N3
eDP_TX_CPU_P2 C5519 SCD1U16V2KX-3DLGP eDP_TX_CON_P2
eDP_TX_CPU_N2 C5520 SCD1U16V2KX-3DLGP eDP_TX_CON_N2
eDP_TX_CPU_P1 C5501 SCD1U16V2KX-3DLGP eDP_TX_CON_P1
eDP_TX_CPU_N1 C5504 SCD1U16V2KX-3DLGP eDP_TX_CON_N1
eDP_TX_CPU_P0 C5506 SCD1U16V2KX-3DLGP eDP_TX_CON_P0
eDP_TX_CPU_N0 C5509 SCD1U16V2KX-3DLGP eDP_TX_CON_N0
3D3V_LCDVDD_S0
NC 3pin for wire
3D3V_CAMERA_S0
3D3V_MIC_VCC
CCD_USB20_CON_P
CCD_USB20_CON_N
DIAGLOOP
R5510 0R0402-PAD
DMIC_SCL_CON
DMIC_SDA_CON
STM-CON40-GP
20.F2406.040
2ND = 020.F1427.0040

M-BIST/ LCD BIST -20180425

LCD BIST for G10 (Was test only for G9)

19V_DCBATOUT_LCD
C5556 SCD1U16V2KX-1DLGP
D5504 RB551V30-GP
83.R5003.H8H
2ND = 83.R5003.T8H
BL_PWR_MONITOR_R
R5532 10KR2J-1-GP
R5533 10KR2J-3-GP
C5557 SC2200P50V2KX-2DLGP
BL_PWR_MONITOR_BJT_B
19V_DCBATOUT
Q5512 MMBT3906-3-GP
BL_PWR_MONITOR_BJT_C
R5534 4K7R2J-2-GP
BL_PWR_MONITOR
3D3V_S5
R5535 100KR2J-1-GP
PANEL_PWRGD
R5558 1MR2J-1-GP
R5536 0R0402-PAD
PANEL_MONITOR
C5558 SCD1U16V2KX-3DLGP
Q5508 LMBT3904LT1G-GP
84.T3904.H11
2ND = 084.03904.0I11
3RD = 084.03904.0H11

3D3V_LCDVDD_S0
C5554 SCD1U16V2KX-3DLGP
D5505 RB551V30-GP
83.R5003.H8H
2ND = 83.R5003.T8H
LCDVDD_MONITOR_R
R5537 10KR2J-1-GP
R5538 10KR2J-3-GP
C5555 SC2200P50V2KX-2DLGP
LCDVDD_MONITOR_BJT_B
3D3V_S0
Q5509 MMBT3906-3-GP
LCDVDD_MONITOR_BJT_C
R5539 4K7R2J-2-GP
LCDVDD_MONITOR
R5540 0R0402-PAD
LCDVDD_MONITOR_BJT_E
Q5510 MBT3904LT1G-GP
84.T3904.H11
2ND = 084.03904.0I11
3RD = 084.03904.0H11

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch
Size: A2
Document Number: NAKIA_SHURI_N7_TGL-U
Rev: A00
Date: Wednesday, August 05, 2020
Sheet 55 of 106

(Blanking)

<Core Design>

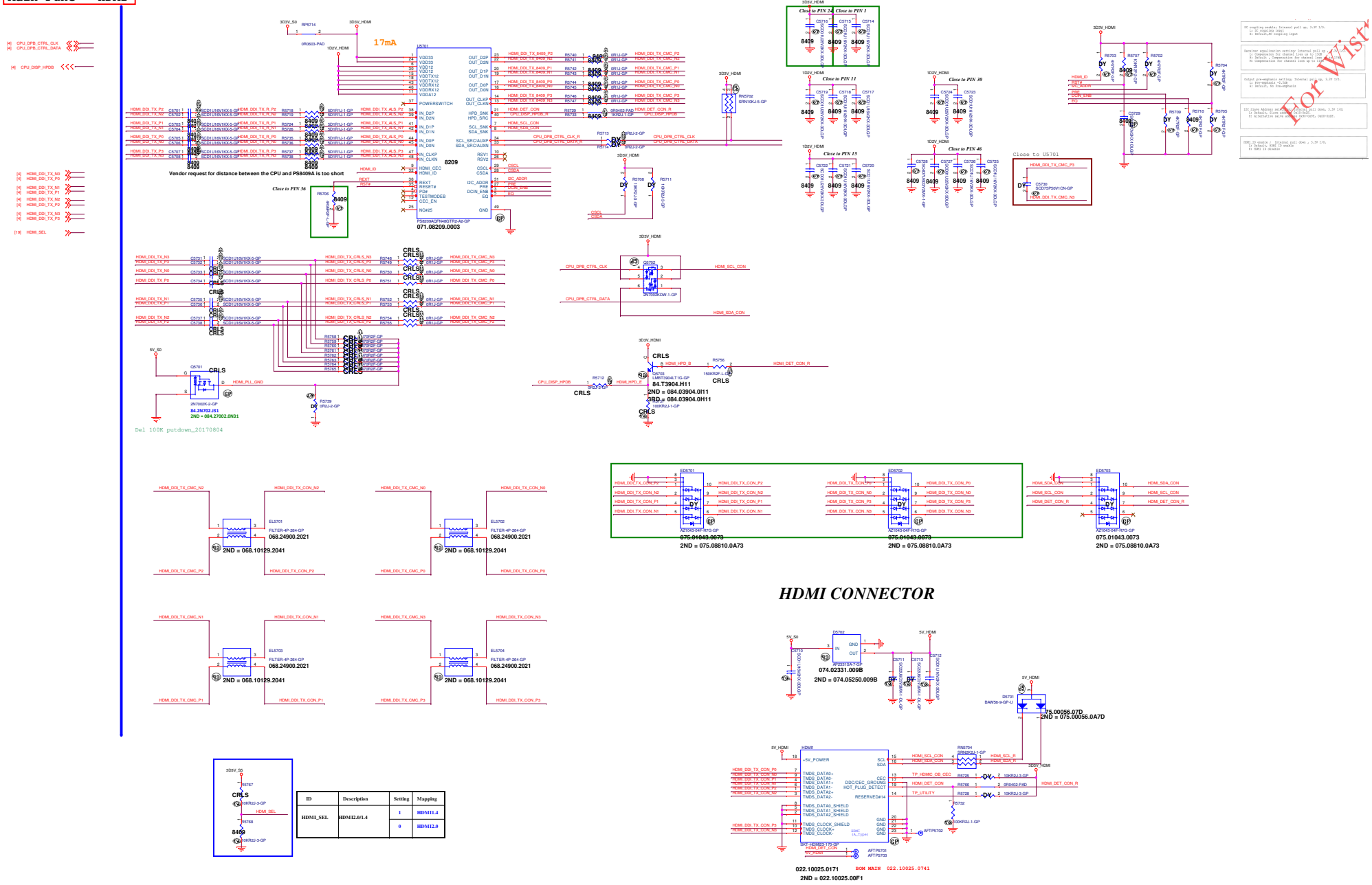
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CRT

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 56 of 106

Main Func = HDMI



ID	Description	Setting	Mapping
HDMI_SEL	HDMI12.0/1.4	1	HDMI1.4
		0	HDMI2.0

For Wistron

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (HDMI Level Shifter/Conn)

Size: A1 | Document Number: Bandon 13' | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 57 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A4	***NAKIA_SHURI_N7_TGL-U***	***A00***

Date: Wednesday, August 05, 2020 Sheet 58 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A4	***NAKIA_SHURI_N7_TGL-U***	

Date: Wednesday, August 05, 2020 Sheet 59 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

SATA IF_HDD/ODD

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 60 of 106

Main Func = WLAN

[16] BT_USB20_P
[16] BT_USB20_N
[16] WLAN_PCIE_TX_P
[16] WLAN_PCIE_TX_N
[16] WLAN_PCIE_RX_P
[16] WLAN_PCIE_RX_N
[18] WLAN_CLK_CPU_N
[18] WLAN_CLK_CPU_P
[18] CLK_PCIE_WLAN_REQ#

[21] CNV_RGI_RSP
[21] CNV_BRI_RSP

[21] CNV_WT_CLKP
[21] CNV_WT_CLKN
[21] CNV_WT_DP0
[21] CNV_WT_DN0
[21] CNV_WT_DP1
[21] CNV_WT_DN1

[21] CNV_WR_CLKP
[21] CNV_WR_CLKN
[21] CNV_WR_DP0
[21] CNV_WR_DN0
[21] CNV_WR_DP1
[21] CNV_WR_DN1

[15,21] CNV_RGI_DT
[21] CNV_BRI_DT
[17,63,71,76,91] PCH_PLTRST#

[21] BT_PCMFRM_RSTN
[21] BT_PCMOUT_CLKREQ0

[19] BT_RADIO_DIS#
[16] WLAN_RF_DIS#

[17] PCIE_WAKE#

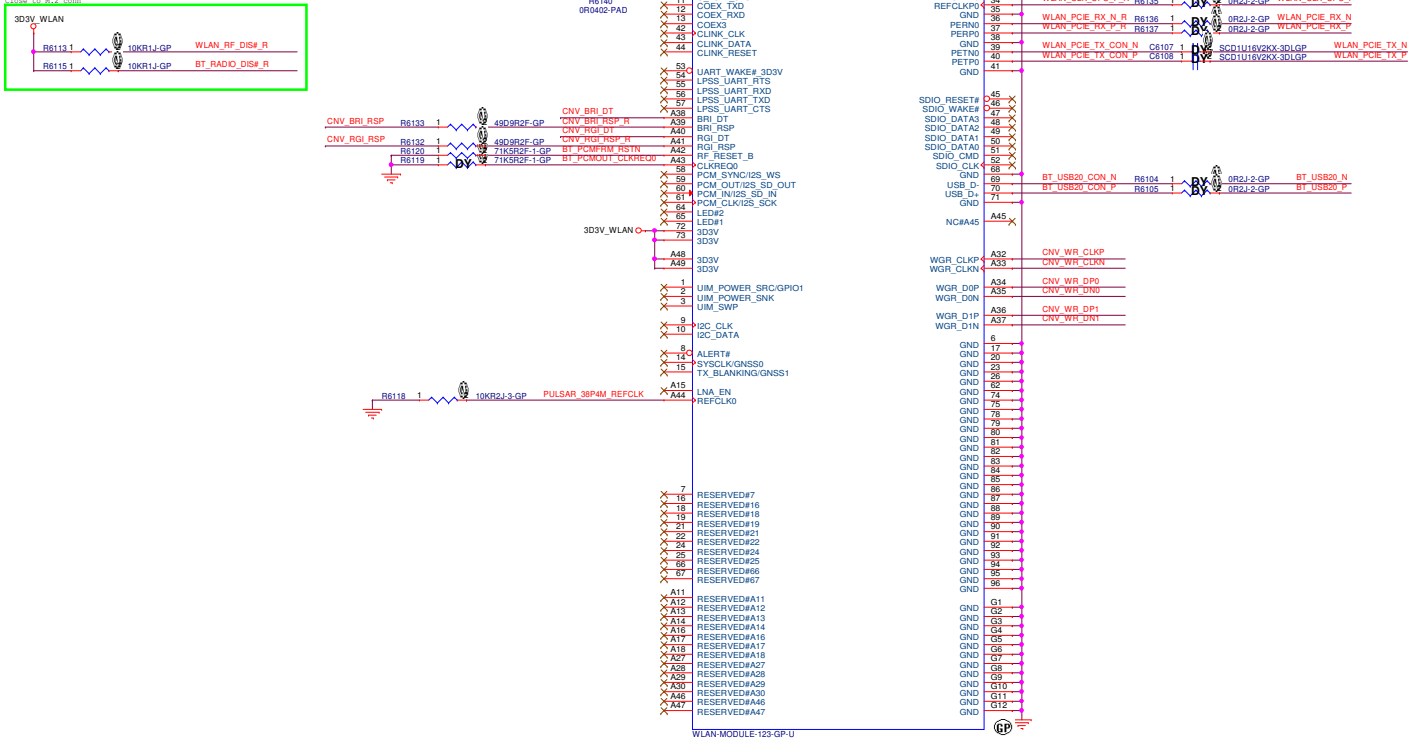
[66] 3D3V_WLAN_P
[66] 3D3V_WLAN_N

[18,24] SUSCLK

C6109~C6111 ,3個電容,靠近WLAN1 pin72&pin73

C6104~C6104,3個電容,靠近WLAN1 pin4&pin5

Layout Note:
Close to M.2 conn



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF_WLAN CONN
Size: A2
Document Number: NAKIA_SHURI_N7_TGL-U
Rev: A00
Date: Wednesday, August 05, 2020
Sheet 61 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

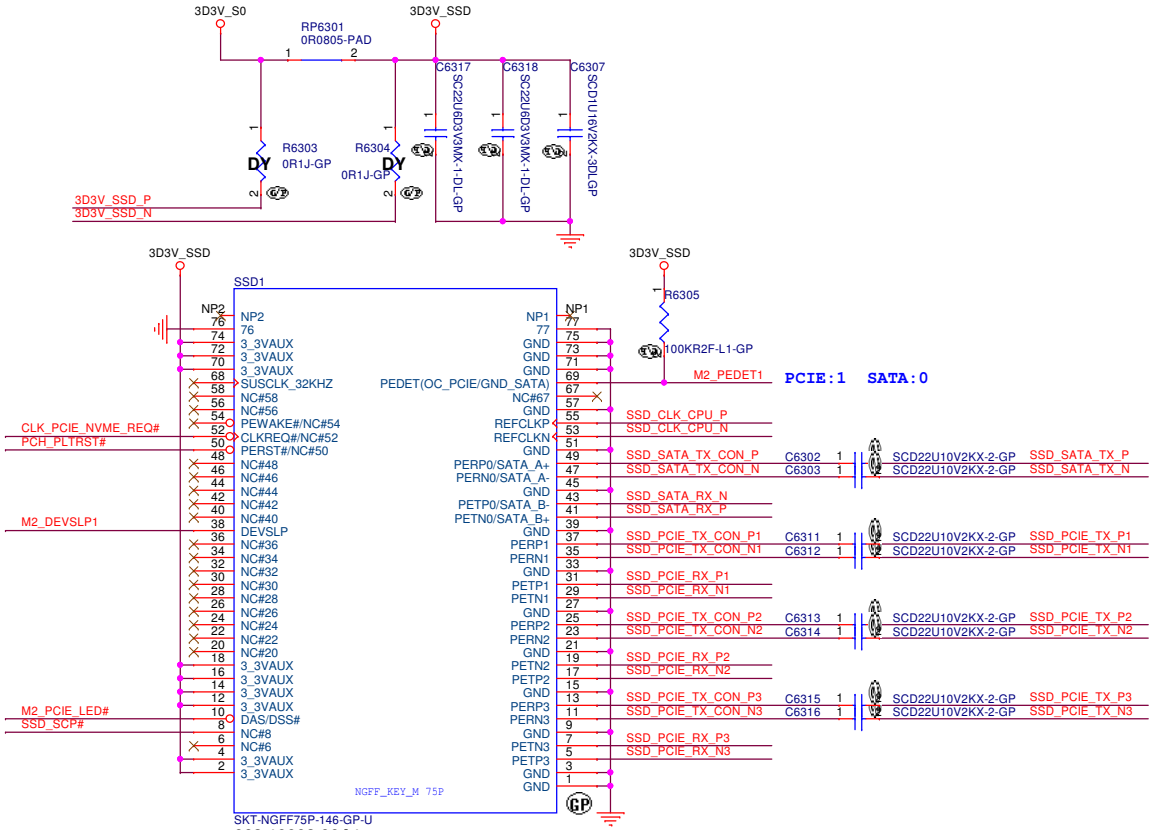
WWAN

Size	Document Number	Rev
A1	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 62 of 106

Main Func = SSD M.2

[16] SSD_PCIE_TX_N3
[16] SSD_PCIE_TX_P3
[16] SSD_PCIE_RX_N3
[16] SSD_PCIE_RX_P3
[16] SSD_PCIE_TX_N2
[16] SSD_PCIE_TX_P2
[16] SSD_PCIE_RX_N2
[16] SSD_PCIE_RX_P2
[16] SSD_PCIE_TX_N1
[16] SSD_PCIE_TX_P1
[16] SSD_PCIE_RX_N1
[16] SSD_PCIE_RX_P1
[16] SSD_SATA_TX_N
[16] SSD_SATA_TX_P
[16] SSD_SATA_RX_N
[16] SSD_SATA_RX_P
[18] SSD_CLK_CPU_P
[18] SSD_CLK_CPU_N
[18] CLK_PCIE_NVME_REQ#
[16] M2_DEVSLP1
[24] SSD_SCP#
[17,61,71,76,91] PCH_PLTRST#
[64] M2_PCIE_LED#
[16] M2_PEDET1
[66] 3D3V_SSD_P
[66] 3D3V_SSD_N



062.10003.00A1
2ND = 062.10003.0991
3RD = 062.10003.0411

Important! SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Table 13-11. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SSD M.2/eMMC

Size: A3 | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00

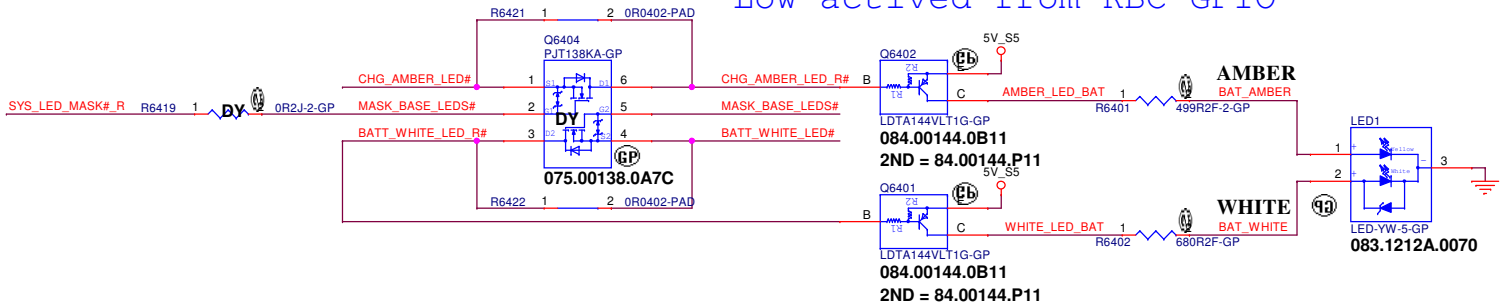
Date: Wednesday, August 05, 2020 | Sheet 63 of 106

Main Func = Power BTN

[24] CHG_AMBER_LED#
[24] BATT_WHITE_LED#
[24] SYS_LED_MASK#_R
[20,24,67,92] ISH_LID_CL#_NB

Battery LED1 (AMBER_LED)

Low actived from KBC GPIO

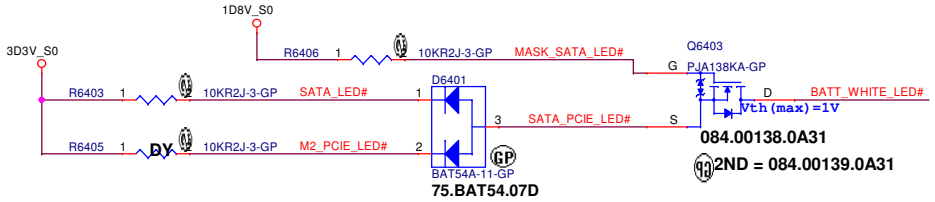


Battery LED2 (WHITE_LED)

Low actived from KBC GPIO

[24] MASK_SATA_LED#
[63] M2_PCIE_LED#
[18] SATA_LED#

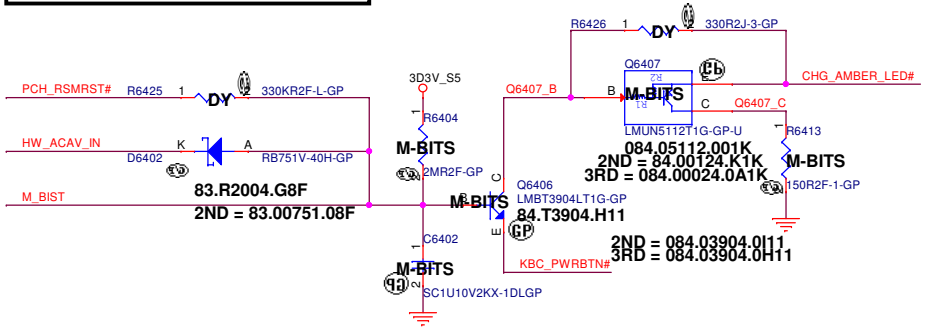
SATA LED



[24,92] KBC_PWRBTN#
[24,44] HW_ACAV_IN
[17,24,40] PCH_RSMRST#
[24] M_BIST

M-BIST for G10

M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Board&Power Button

Size	Document Number	Rev
A3	NAKIA SHURI N7 TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 64 of 106

Main Func = Keyboard

[24] KSO00
[24] KSO01
[24] KSO02
[24] KSO03
[24] KSO04
[24] KSO05
[24] KSO06
[24] KSO07
[24] KSO08
[24] KSO09
[24] KSO10
[24] KSO11
[24] KSO12
[24] KSO13
[24] KSO14
[24] KSO15
[24] KSO16

[24] KSI00
[24] KSI01
[24] KSI02
[24] KSI03
[24] KSI04
[24] KSI05
[24] KSI06
[24] KSI07

[4] KB_DET#
[24] KB_LED_PWM
[24] CAP_LED#_R
[20] KB_LED_BL_DET

285mA max.

5V_S0
5V_KB_BL
F6501
POLYSW-1D1A6V-9-GP-U
69.48001.081
2ND = 69.50011.081
C6501
SCD1U16V2KX-3DLGP
KB_LED_BL_DET
R6507 51KR2J-1-GP
R6508 100KR2J-1-GP
C6504 SCD1U16V2KX-3DLGP
DY
KB_LED_DET_C
KB_BL_CTRL#
KBBL1
ACES-CON4-90-GP-U
020.K0298.0004
2ND = 020.K0311.0004
Q6501
PJA3402-R1-00001-GP
084.03402.0031
2ND = 084.02306.0031
KB_LED_PWM
R6509 100KR2J-1-GP
AFTP6530
AFTP6529
AFTP6540
KB_BL_CTRL#
5V_KB_BL
KB_LED_DET_C

5V_S5
LOW actived from KBC GPIO
Q6505
LDTA144VLT1G-GP
CAP_LED#_R
CAP_LED_Q
R6513 1KR2J-1-GP
CAP_LED
084.00144.0B11
2ND = 84.00144.P11
KB1
CAP_LED
AFTP6538
AFTP6523
AFTP6522
AFTP6504
AFTP6521
AFTP6520
AFTP6524
AFTP6539
AFTP6519
AFTP6507
AFTP6513
AFTP6511
AFTP6518
AFTP6516
AFTP6517
AFTP6515
AFTP6514
AFTP6510
AFTP6512
AFTP6509
AFTP6501
AFTP6506
AFTP6508
AFTP6505
AFTP6503
AFTP6502
KSO10
KSO11
KSO09
KSO14
KSO13
KSO15
KSO16
KSO12
KSO00
KSO01
KSO02
KSO03
KSO08
KSO06
KSO07
KSO04
KSO05
KSI00
KSI03
KSI01
KSI05
KSI02
KSI04
KSI06
KSI07
KB_DET#
ACES-CON30-29-GP
020.K0254.0030
2ND = 20.K0750.030
3RD = 020.K0274.0030

Main Func = TPAD

TP to EC/PD

[24] EC_I2C2_SDA_TP
[24] EC_I2C2_SCL_TP

TP to PCH

[20,66] PCH_I2C1_SDA_TP
[20,66] PCH_I2C1_SCL_TP

[24] PTP_DIS#
[3,24] TOUCH_PAD_INTR#

3D3V_TP_VDD
RN6504 SRN2K2J-7-GP
I2C_SDA_TP
I2C_SCL_TP
R6511 10KR2J-3-GP
TOUCH_PAD_INTR#
Need to check if it is Active High or Active Low
and check if there is PH on TPAD side.

3D3V_S0
3D3V_S5
3D3V_TP_VDD
RP6502 0R0603-PAD
R6503 DY 0R2J-2-GP
C6505 SCD1U16V2KX-3DLGP
TPAD1

I2C to EC
EC_I2C2_SDA_TP
EC_I2C2_SCL_TP
RN6502 SRN0J-6-GP
I2C_SDA_TP
I2C_SCL_TP

TOUCH_PAD_INTR#
PTP_DIS#

I2C to PCH
PCH_I2C1_SCL_TP
PCH_I2C1_SDA_TP
RN6503 SRN0J-6-GP

020.K0255.0008
2ND = 020.K0151.0008

3D3V_TP_VDD
AFTP6531
TOUCH_PAD_INTR#
PTP_DIS#
AFTP6536
AFTP6537
AFTP6525

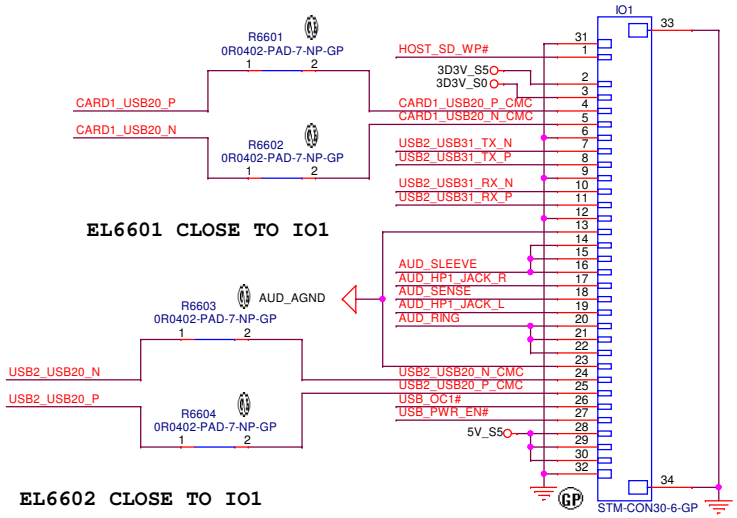
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board&Touch Pad
Size: A3
Document Number: NAKIA_SHURI_N7_TGL-U
Rev: A00
Date: Wednesday, August 05, 2020
Sheet 65 of 106

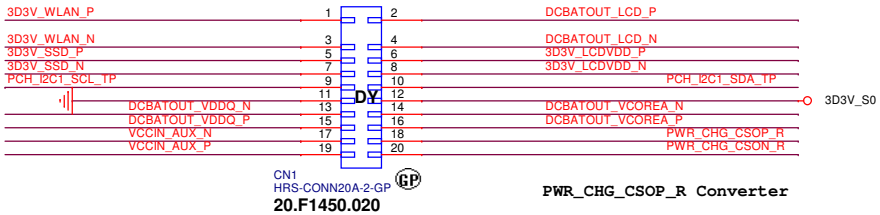
Main Func = IO Connector

[16] USB2_USB31_TX_P
[16] USB2_USB31_TX_N
[16] USB2_USB31_RX_P
[16] USB2_USB31_RX_N
[16] USB2_USB20_N
[16] USB2_USB20_P
[24,35] USB_PWR_EN#
[4] USB_OC1#
[16] CARD1_USB20_N
[16] CARD1_USB20_P
[18] HOST_SD_WP#
[27,29] AUD_HP1_JACK_L
[27,29] AUD_HP1_JACK_R
[27,29] AUD_SLEEVE
[27,29] AUD_RING
[27] AUD_SENSE



020.F1027.0030
2ND = 20.F2056.030
3RD = 020.F1428.0030

[44] PWR_CHG_CSOP_R
[44] PWR_CHG_CSON_R
[20,65] PCH_I2C1_SDA_TP
[20,65] PCH_I2C1_SCL_TP
[61] 3D3V_WLAN_N
[61] 3D3V_WLAN_P
[63] 3D3V_SSD_N
[63] 3D3V_SSD_P
[51] DCBATOUT_VDDQ_P
[51] DCBATOUT_VDDQ_N
[50] VCCIN_AUX_P
[50] VCCIN_AUX_N
[55] DCBATOUT_LCD_P
[55] DCBATOUT_LCD_N
[47] DCBATOUT_VCOREA_P
[47] DCBATOUT_VCOREA_N
[55] 3D3V_LCDVDD_P
[55] 3D3V_LCDVDD_N



20.F1450.020

PWR_CHG_CSOP_R Converter

<Core Design>

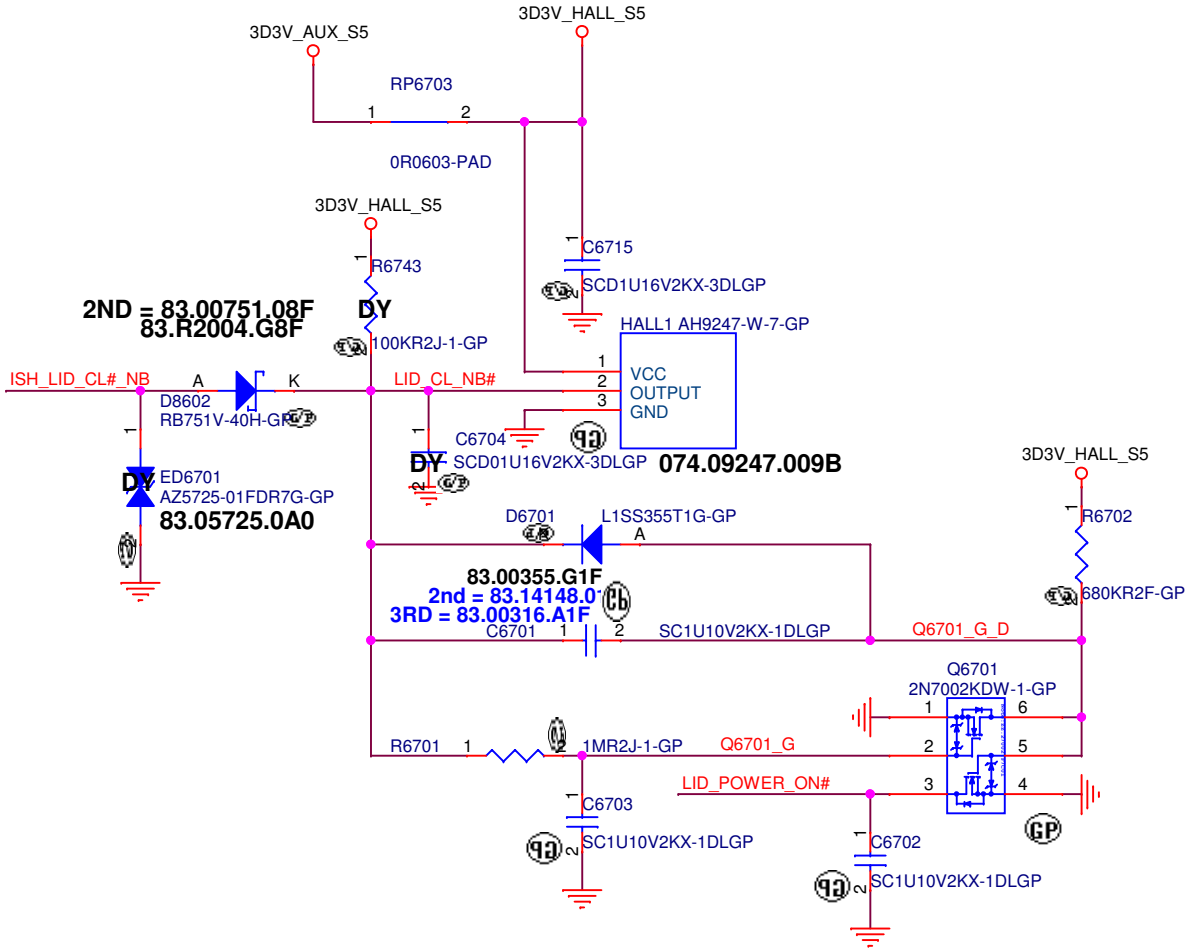
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector
Size: A3
Document Number: NAKIA SHURI N7 TGL-U
Rev: A00
Date: Wednesday, August 05, 2020
Sheet 66 of 106

Main Func = HALL SENSOR

[20,24,92] ISH_LID_CL#_NB

[24] LID_POWER_ON#



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Sensor (Hall-Sensor)***

Size	Document Number	Rev
A4	***NAKIA_SHURI_N7_TGL-U***	***A00***

Date: Wednesday, August 05, 2020 Sheet 67 of 106

Main Func = Debug

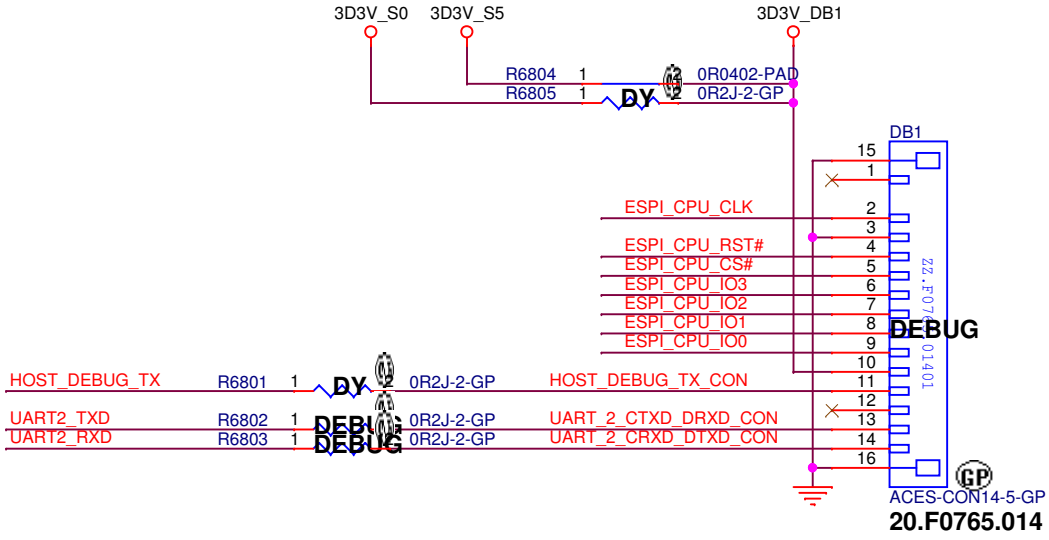
[18,24] ESPI_CPU_IO0
[18,24] ESPI_CPU_IO1
[18,24] ESPI_CPU_IO2
[18,24] ESPI_CPU_IO3

[18,24] ESPI_CPU_RST#
[18,24] ESPI_CPU_CS#
[18,24] ESPI_CPU_CLK

[24] HOST_DEBUG_TX

[20] UART2_TXD

[20] UART2_RXD



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Dubug connector*

Size	Document Number	Rev
A4	*NAKIA_SHURI_N7_TGL-U*	*A00*

Date: Wednesday, August 05, 2020 Sheet 68 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	*NAKIA_SHURI_N7_TGL-U*	*A00*

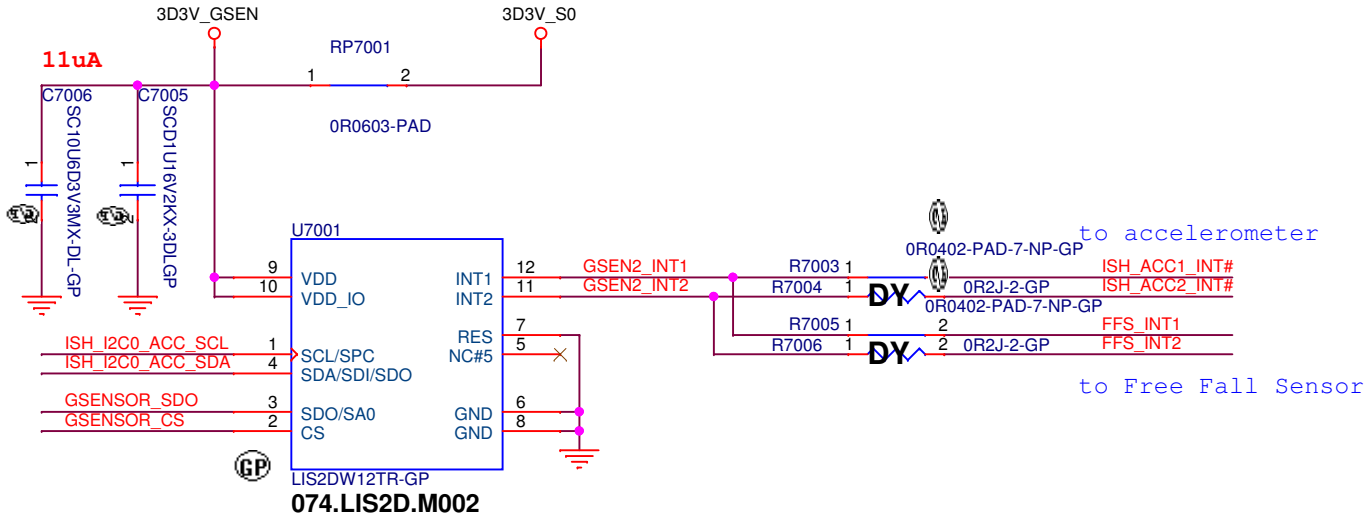
Date: Wednesday, August 05, 2020 Sheet 69 of 106

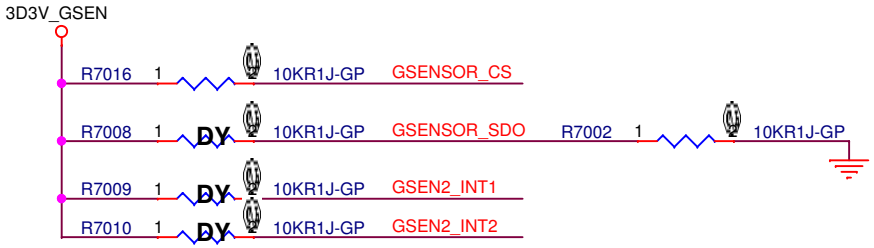
Main Func = G-sensor

[20] ISH_ACC1_INT#
[20] ISH_ACC2_INT#

[20] FFS_INT1
[19] FFS_INT2

[20] ISH_I2C0_ACC_SCL
[20] ISH_I2C0_ACC_SDA





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Sensor**

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 70 of 106

Main Func = TBT

HP team on applying, only murata have sample can meet Intel request

220nF AC cap must be placed on RX lines close to SOC side

HP team on applying ,only murata have sample can meet Intel request

TBT PORTS

U7101D

ZZ.000IC.002

MISC & DEBUG

U7101A

ZZ.000IC.002

BB TO PD

BB TO PCH(TBT)

BB TO PCH(NON-TBT)

2ND = 082.30005.0C81

Power

U7101B

ZZ.000IC.002

GND

U7101C

ZZ.000IC.002

U7103

072.25Q80.0C01

U7102

2ND = 74.03526.093

USB1

Type-C PD

PCH to BB

BB Strap PIN

	BB_TCP1_FLASH_SHARE_EN	BB_TCP1_FLASH_MSTR_SLV
H	FLASH SHARE ENABLE	MASTER MODE
L	FLASH SHARE DISABLE	SLAVE MODE

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

EXT IO (Thunderbolt(1/3)/Type C Re-driver)

NAKIA_SHURI_N7_TGL-U

A00

Wednesday, August 05, 2020

Main Func = TypeC MUX

PD to EC/TP

[24] UPD1_SMBINT#
[24] UPD1_SMBDAT
[24] UPD1_SMBCLK

PD To PCH

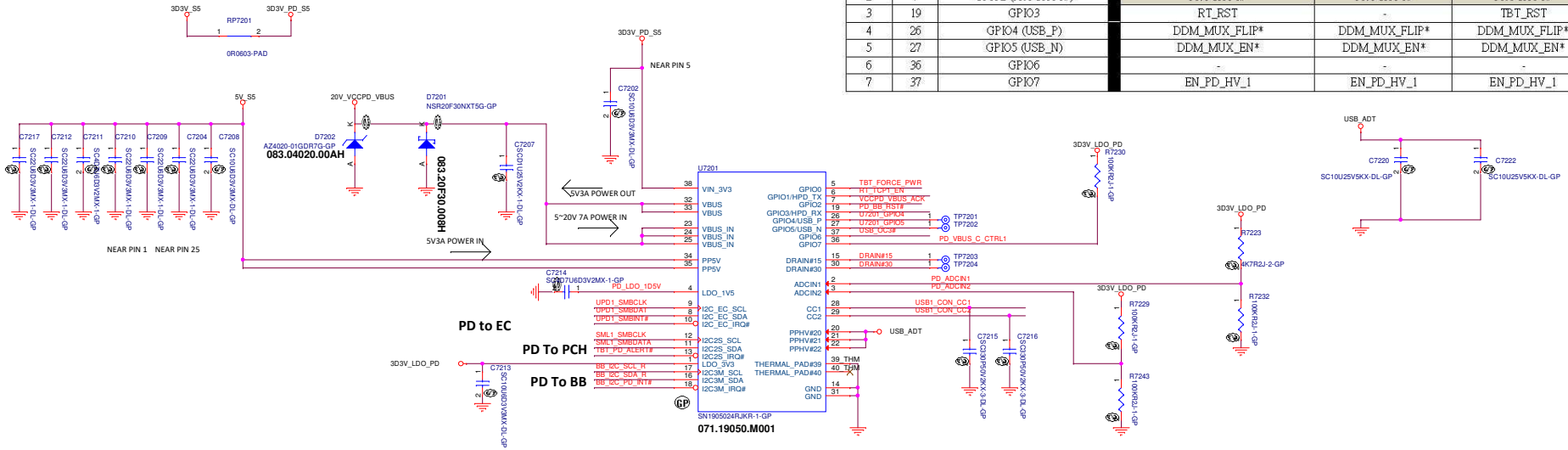
[17] TBT_PD_ALERT#

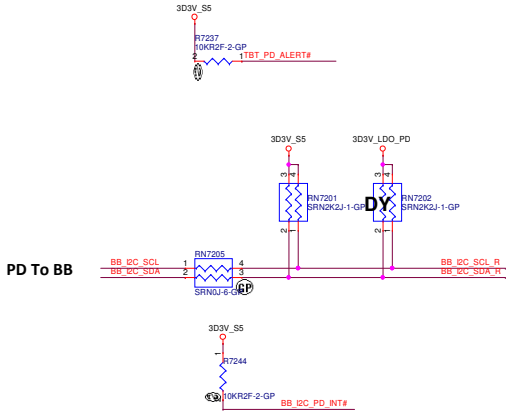
PD To BB

[71] BB_I2C_SCL
[71] BB_I2C_SDA
[71] BB_I2C_PD_INT#
[71] PD_BB_RST#
[16,71] TBT_FORCE_PWR
[71] RT_TCP1_EN
[44] VCCPD_VBUS_ACK
[74] PD_VBUS_C_CTRL
[16] USB_OC3#

[16] USB3_USB20_P
[16] USB3_USB20_N
[73] USB1_CON_CC1
[73] USB1_CON_CC2
[18] SML1_SMBCLK
[18] SML1_SMBDATA
[73] TOP_MUX_P_L
[73] TOP_MUX_N_L
[73] BOT_MUX_P_L
[73] BOT_MUX_N_L

GPIO	Pin #	Package Pin Name	TPS65992D		
			TGL w/ Burnside Bridge RT	RKL w/o TBT	RKL w/ TR or MR
0	5	GPIO0	RT_FORCE_PWR	-	-
1	6	GPIO1 (HPD_Tx)	RT_EN	HPD_Tx	-
2	7	GPIO2 (PROCHOT#)	PROCHOT#	PROCHOT#	PROCHOT#
3	19	GPIO3	RT_RST	-	TBT_RST
4	26	GPIO4 (USB_P)	DDM_MUX_FLIP*	DDM_MUX_FLIP*	DDM_MUX_FLIP*
5	27	GPIO5 (USB_N)	DDM_MUX_EN*	DDM_MUX_EN*	DDM_MUX_EN*
6	36	GPIO6	-	-	-
7	37	GPIO7	EN_PD_HV_1	EN_PD_HV_1	EN_PD_HV_1





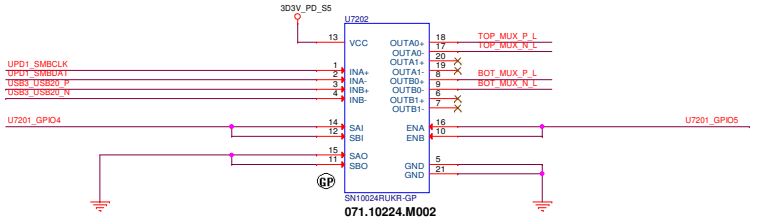


Table 2. Decoding of ADCIN1 and ADCIN2 Pins

$DIV = R_{DOWN} / (R_{UP} + R_{DOWN})$ (1)			Without using R_{UP} or R_{DOWN}	ADCINx decoded value
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.8062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO_3V3	7

Confidential

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (Thunderbolt(2/3)/Type C CC Logic)

Size: A2 | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 72 of 106

Main Func = Type-C Port1

[71] USB1_SSTX_CON_P0
[71] USB1_SSTX_CON_N0
[71] USB1_SSTX_CON_P1
[71] USB1_SSTX_CON_N1

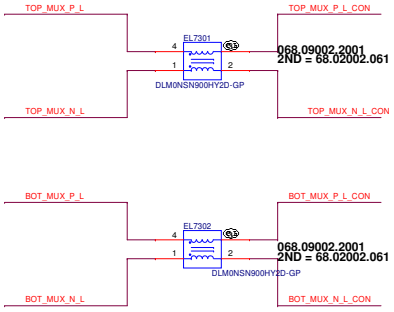
[71] USB1_SSRX_CON_P0
[71] USB1_SSRX_CON_N0
[71] USB1_SSRX_CON_P1
[71] USB1_SSRX_CON_N1

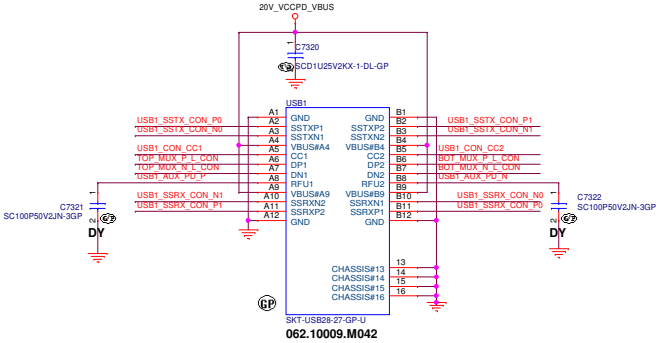
[71] USB1_AUX_PD_P
[71] USB1_AUX_PD_N

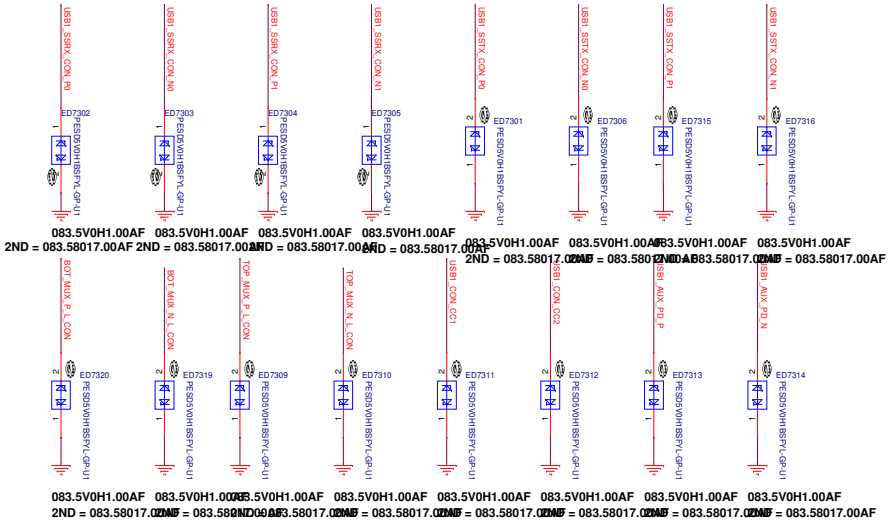
[72] USB1_CON_CC1
[72] USB1_CON_CC2

[72] TOP_MUX_P_L
[72] TOP_MUX_N_L

[72] BOT_MUX_P_L
[72] BOT_MUX_N_L







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (Thunderbolt(3/3)/Type C Conn)

Size	Document Number	Rev
A2	NAKIA_SHURI_N7_TGL-U	A00

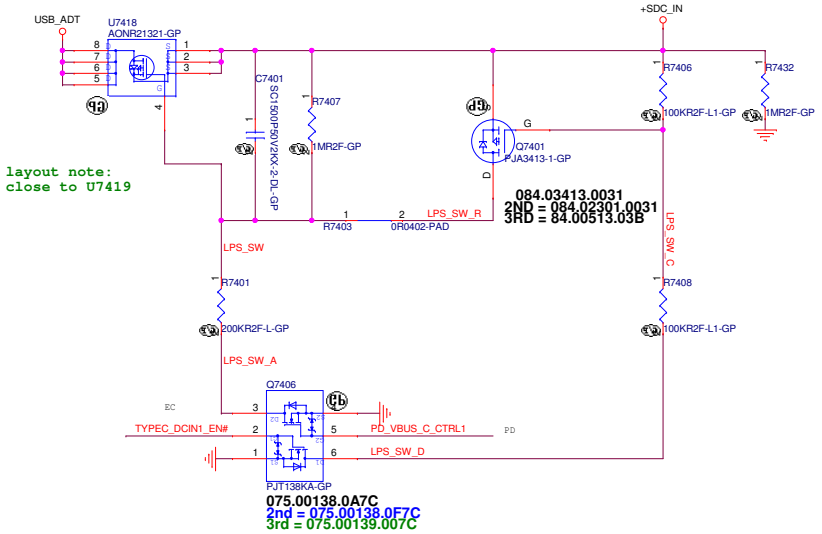
Date: Wednesday, August 05, 2020 Sheet 73 of 106

Main FUNC = LPS

CCG5_ILIM#	ILIM
0	1.5A
1	3.3A

[24] TYPEC_DCIN1_EN#

[72] PD_VBUS_C_CTRL1



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(2/5)DIGITALOUT

Size	Document Number	Rev
Custom	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 74 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)Thunderbolt (5/5)

Size	Document Number	Rev
A2	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 75 of 106

Main Func = dGPU

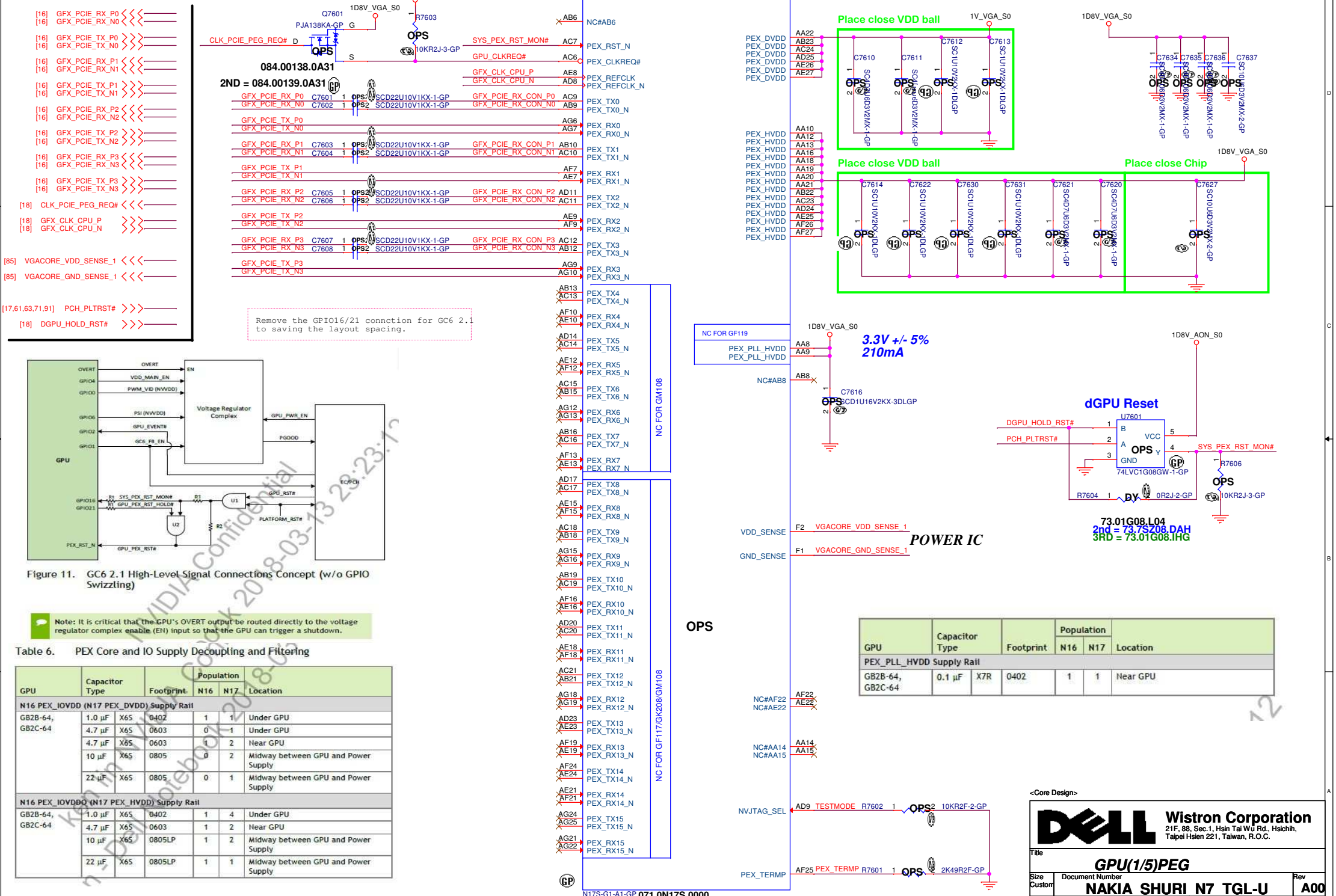


Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

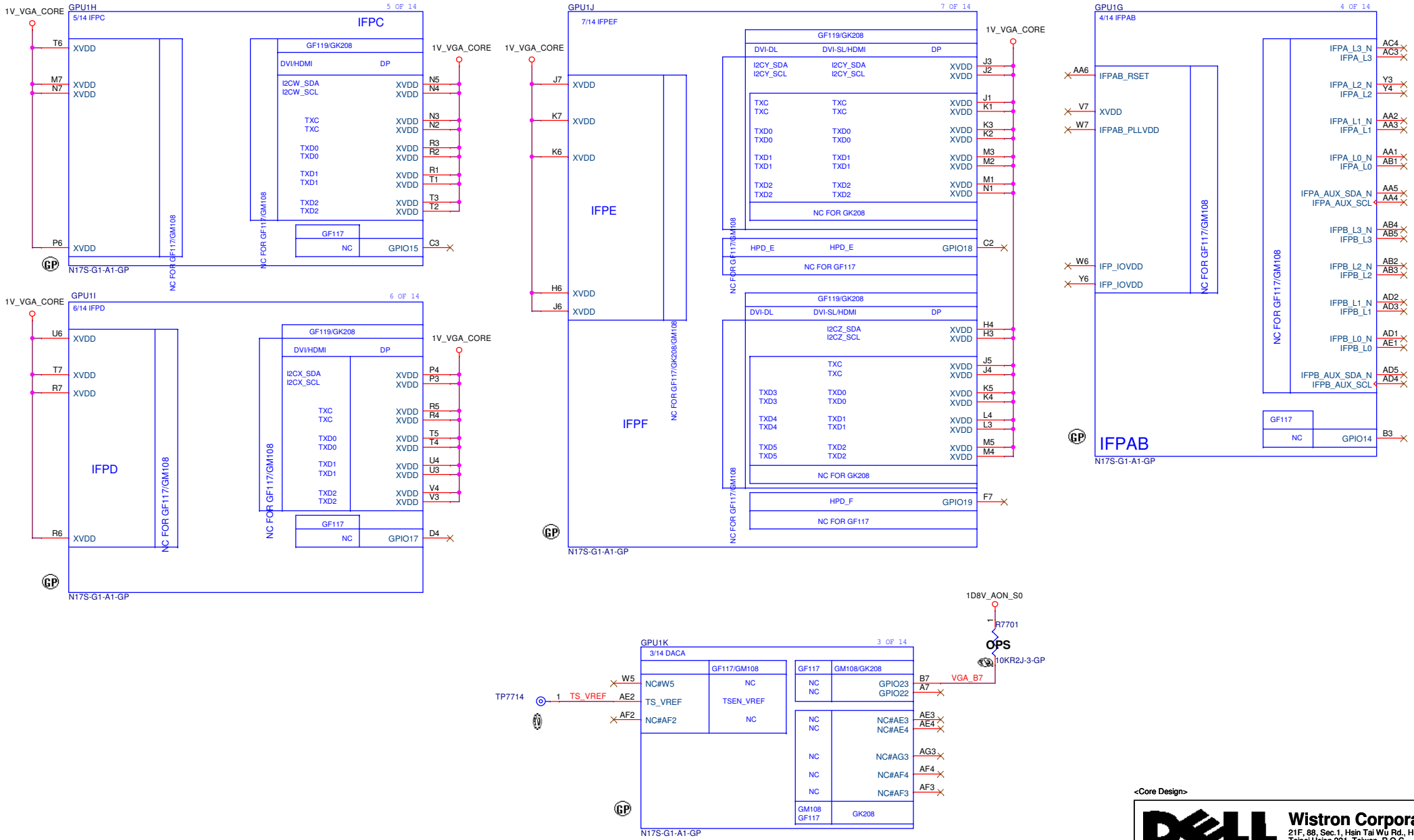
GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

NVIDIA Confidential
Compal 2018-03-13 28:23:1
Kenin_Dell Notebook 2018-03

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(1/5)PEG
Size: Custom | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00
Date: Wednesday, August 05, 2020 | Sheet 76 of 106

Main Func = dGPU



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(2/5)DIGITALOUT

Size	Document Number	Rev
A3	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 77 of 106

Main Func = dGPU

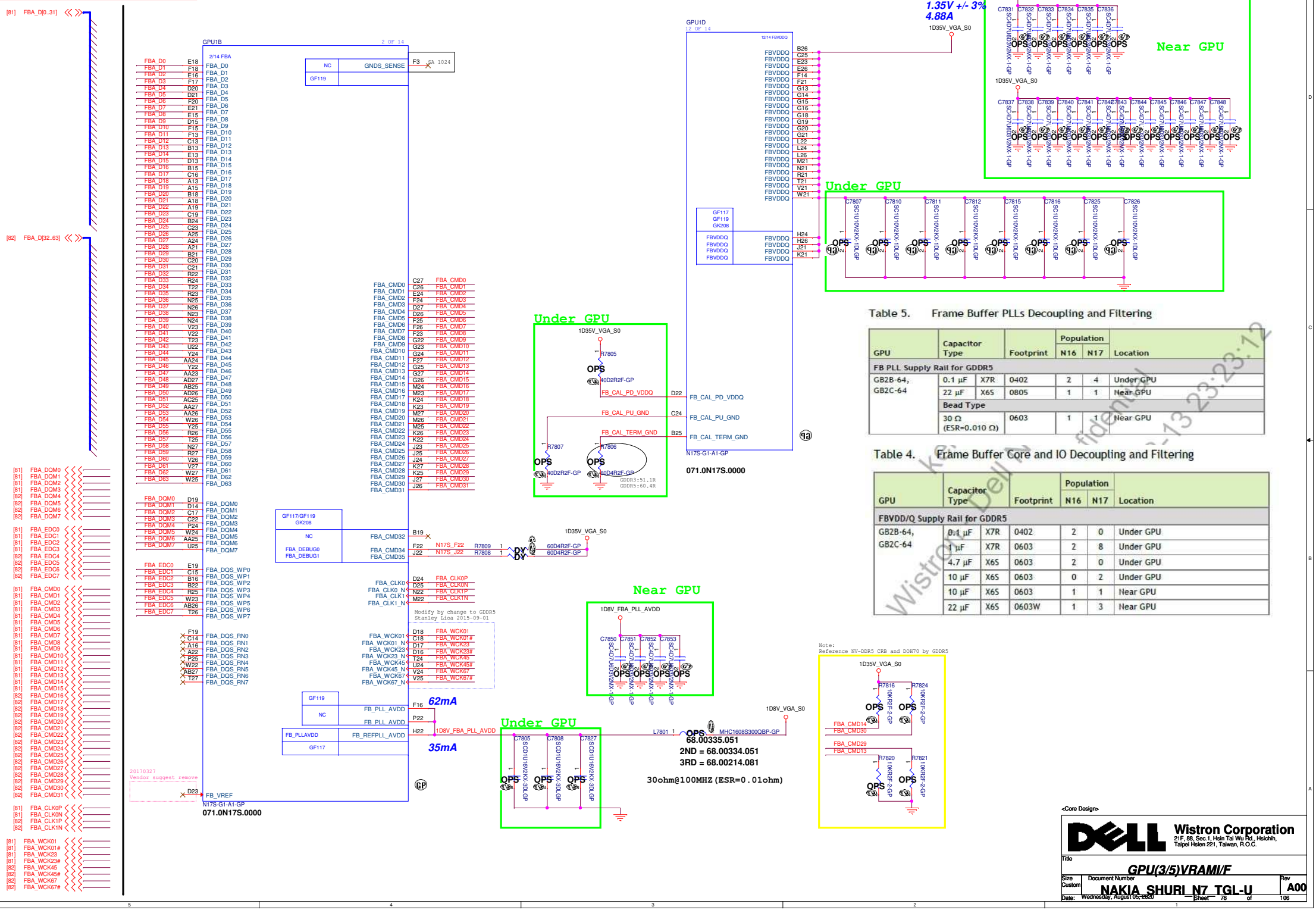


Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

Wistron Dell fidential k 2017-03-13 23:23:12

<Core Design>

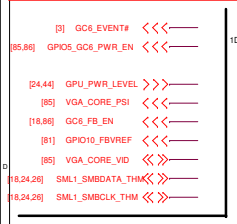
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

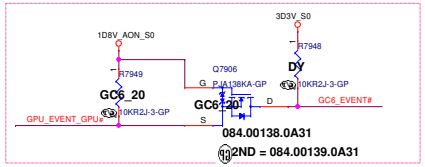
Title: GPU(3/5)VRAM/F

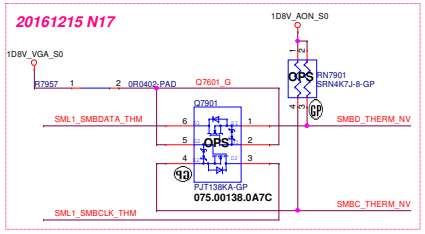
Size: Custom | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00

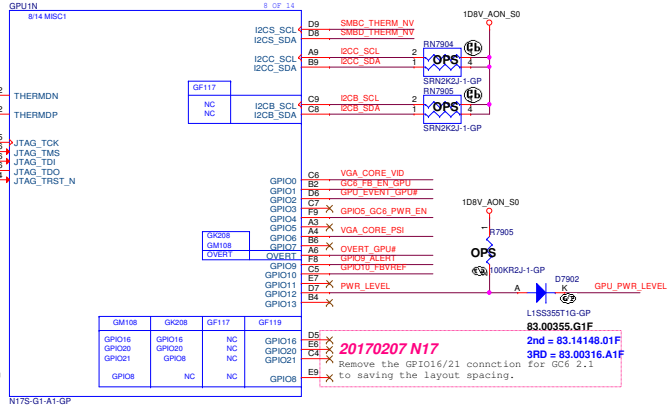
Date: Wednesday, August 05, 2020 | Sheet 78 of 106

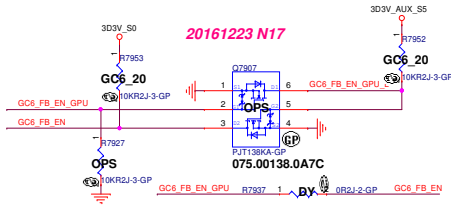
Main Func = dGPU

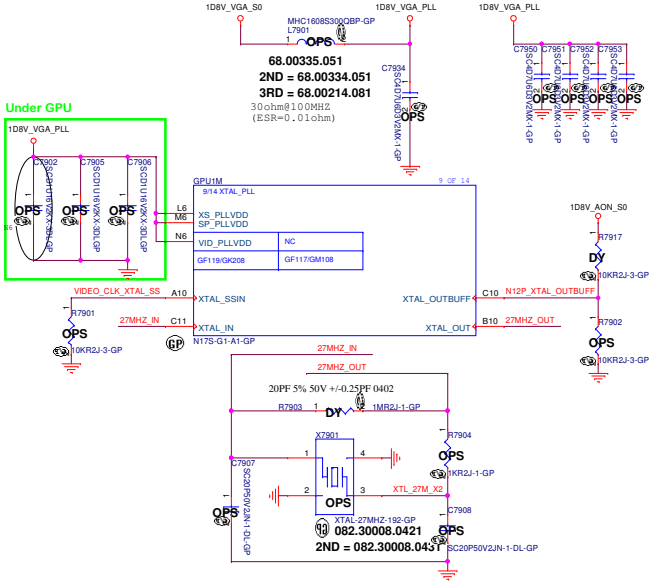




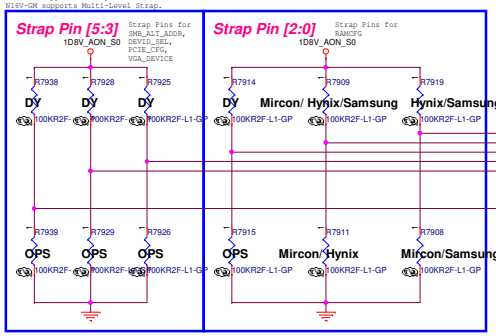


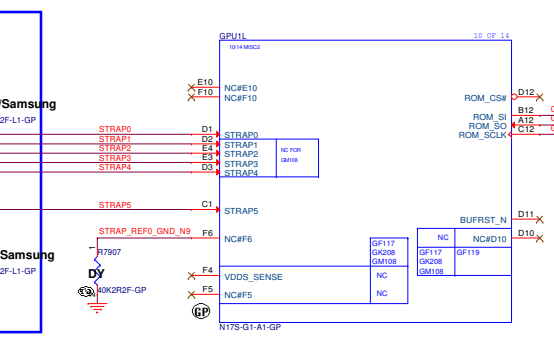






N15V-GS supports Binary Mode.
N16V-GM supports Multi-Level Strap.





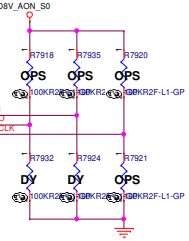


Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
H	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009) Micron
L	M	H	10 (0x000A) Hynix
L	H	M	11 (0x000B) Samsung
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 4. N17S-G5/LP GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production candidate
			Samsung	K4G80325FC-HC25	C-die	0x8	8 Gbps	N/A	Full	Production candidate

Notes:
1. For N17S-G5/LP, the maximum allowable memory case temperature is 85 °C.

Cheng Wu NVIDIA confidential
Cheng Wu NVIDIA confidential 2019-12-29 23:

<Core Design>

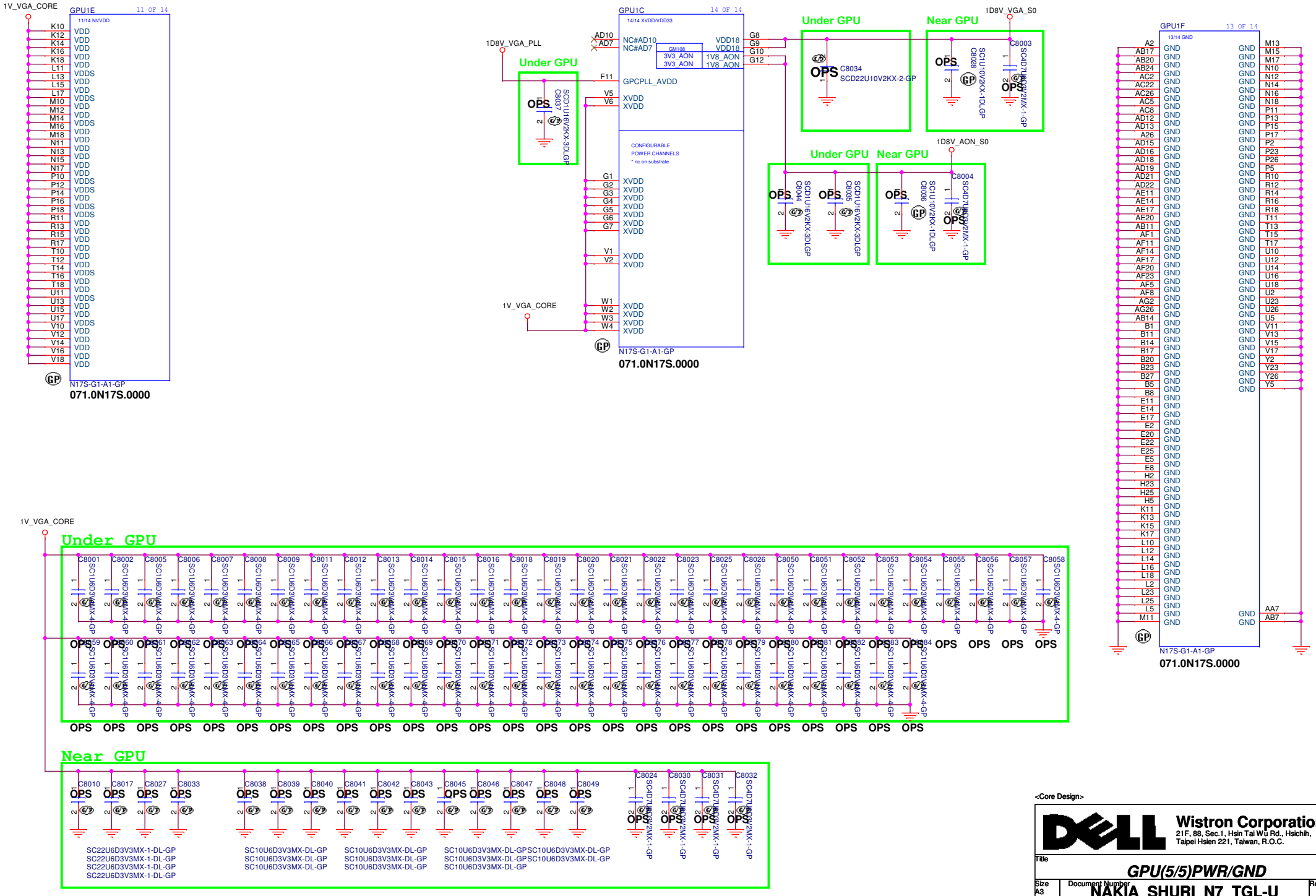
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(4/5)GPIO/STRAP

Size: A2 | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 79 of 106

Main Func = dGPU



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(5/5)PWR/GND

Size	Document Number	Rev
A3	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 80 of 106

SSID = VRAM

[78,81] FBA_CMD6
[78,81] FBA_CMD11
[78,81] FBA_CMD10
[78,81] FBA_CMD7
[78,81] FBA_CMD9

[78,81] FBA_CMD2
[78,81] FBA_CMD4
[78,81] FBA_CMD3
[78,81] FBA_CMD1

[78,81] FBA_CMD8
[78,81] FBA_CMD12
[78,81] FBA_CMD0
[78,81] FBA_CMD15
[78,81] FBA_CMD5

[78] FBA_CLK0P
[78] FBA_CLK0N
[78,81] FBA_CMD14

[82] FBA_VREFC0

[78,81] FBA_CMD13

[79] GPIO10_FBVREF

[78,81] FBA_D[0..31]

[78,81] FBA_D[0..31]

[78,81] FBA_CMD10
[78,81] FBA_CMD7
[78,81] FBA_CMD6
[78,81] FBA_CMD11
[78,81] FBA_CMD9

[78,81] FBA_CMD3
[78,81] FBA_CMD1
[78,81] FBA_CMD2
[78,81] FBA_CMD4

[78,81] FBA_CMD8
[78,81] FBA_CMD15
[78,81] FBA_CMD5
[78,81] FBA_CMD12
[78,81] FBA_CMD0

[78,81] FBA_D[0..31]

[78,81] FBA_D[0..31]

[78] FBA_DQM0
[78] FBA_DQM1
[78] FBA_DQM2
[78] FBA_DQM3

[78] FBA_EDC0
[78] FBA_EDC1
[78] FBA_EDC2
[78] FBA_EDC3

[78] FBA_WCK23
[78] FBA_WCK23#
[78] FBA_WCK01
[78] FBA_WCK01#

[78,81] FBA_CMD14

[78,81] FBA_CMD13

1D35V_VGA_S0

VRAM1A 1 OF 2

C5 C10 D11 G1 G4 G11 G14 L1 L4 L11 L14 P11 R5 R10 — VDD

B1 B3 B12 B14 D1 D3 D12 D14 E5 E10 F1 F3 F12 F14 G2 G13 H3 H12 K3 K12 L2 L13 M1 M3 M12 M14 N5 N10 P1 P3 P12 P14 T1 T3 T12 T14 — VDDQ

B5 B10 D10 G5 G10 H1 H14 K1 K14 L5 L10 P10 T5 T10 — VSS

A1 A3 A12 A14 C1 C3 C4 C11 C12 C14 E1 E3 E12 E14 F5 F10 H2 H13 K2 K13 M5 M10 N1 N3 N12 N14 R1 R3 R4 R11 R12 R14 U1 U3 U12 U14 — VSSQ

OPS

FBA_VREFC0 J14 — VREFC

A10 VREFD
U10 VREFD

VPP/NC#A5 A5
VPP/NC#U5 U5

OPS C8126 SC820P50V2KX-1-DL-GP

H5GQ2H24AFR-T2C-GP

72.05224.A0U

Frame Buffer Patition A-Lower Half

1D35V_VGA_S0

R8106 549R2F-GP OPS

FBA_VREFC0

R8107 1K33R2F-GP OPS

R8104 931R2F-1-GP OPS

FBA_VREF_FET_L

Q8101 PJA138KA-GP OPS GP

G S D

084.00138.0A31
2ND = 084.00139.0A31

GPIO10_FBVREF

FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

Normal(MF=0)

VRAM1B 2 OF 2

FBA_CMD6 K4
FBA_CMD11 H5
FBA_CMD10 H4
FBA_CMD7 K5
FBA_CMD9 J5

FBA_CMD2 H11
FBA_CMD4 K10
FBA_CMD3 K11
FBA_CMD1 H10

FBA_CMD8 J4
FBA_CMD12 G3
FBA_CMD0 G12
FBA_CMD15 L3
FBA_CMD5 L12

FBA_CLK0P J12
FBA_CLK0N J11
FBA_CMD14 J3

FBA_DQM0 D2
FBA_DQM1 D13
FBA_DQM2 P13
FBA_DQM3 P2

FBA_CMD13 J2

FBA_SEN0 J10
FBA_ZQ0 J13
FBA_MF1 J1

FBA_WCK01 D4
FBA_WCK01# D5

FBA_WCK23 P4
FBA_WCK23# P5

A8/A7 A9/A1 A10/A0 A11/A6 A12/RFU#J5/NC#J5
BA0/A2 BA1/A5 BA2/A4 BA3/A3
ABI# RAS# CS# CAS# WE#
CK CK# CKE#
DBI0# DBI1# DBI2# DBI3#
RESET#
SEN ZQ MF
WCK01 WCK01#
WCK23 WCK23#

OPS

DQ0 A4 FBA_D0
DQ1 A2 FBA_D1
DQ2 B4 FBA_D2
DQ3 B2 FBA_D3
DQ4 E4 FBA_D4
DQ5 E2 FBA_D5
DQ6 F4 FBA_D6
DQ7 F2 FBA_D7
DQ8 A11 FBA_D8
DQ9 A13 FBA_D9
DQ10 B11 FBA_D10
DQ11 B13 FBA_D11
DQ12 E11 FBA_D12
DQ13 E13 FBA_D13
DQ14 F11 FBA_D14
DQ15 F13 FBA_D15
DQ16 U11 FBA_D16
DQ17 U13 FBA_D17
DQ18 T11 FBA_D18
DQ19 T13 FBA_D19
DQ20 N11 FBA_D20
DQ21 N13 FBA_D21
DQ22 M11 FBA_D22
DQ23 M13 FBA_D23
DQ24 U4 FBA_D24
DQ25 U2 FBA_D25
DQ26 T4 FBA_D26
DQ27 T2 FBA_D27
DQ28 N4 FBA_D28
DQ29 N2 FBA_D29
DQ30 M4 FBA_D30
DQ31 M2 FBA_D31

EDC0 C2 FBA_EDC0
EDC1 C13 FBA_EDC1
EDC2 R13 FBA_EDC2
EDC3 R2 FBA_EDC3

H5GQ2H24AFR-T2C-GP

R8110 0R0402-PAD
R8108 121R2F-GP OPS
R8111 1KR2J-1-GP OPS

FBA_CLK0N
FBA_CLK0P

R8102 40D2R2F-GP OPS
R8101 40D2R2F-GP OPS

FBA_CLK0_MIDPT

C8101 SCD01U25V2KX-3DLGP OPS

Place close VDD ball

1D35V_VGA_S0

C8104 SC10U6D3V3MX-DL-GP OPS

1D35V_VGA_S0

C8105 C8106 C8107 C8109 OPS

SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP

1D35V_VGA_S0

C8108 C8115 C8120 C8121 C8122 C8123 C8124 C8125 OPS DY

SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP

SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP

Place close VDDQ ball

1D35V_VGA_S0

C8113 SC10U6D3V3MX-DL-GP OPS

1D35V_VGA_S0

C8110 C8111 C8112 C8114 OPS

SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP
SC1U10V2KX-1DLGP

1D35V_VGA_S0

C8116 C8117 C8118 C8119 OPS

SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP
SCD1U16V2KX-3DLGP

<Core Design>

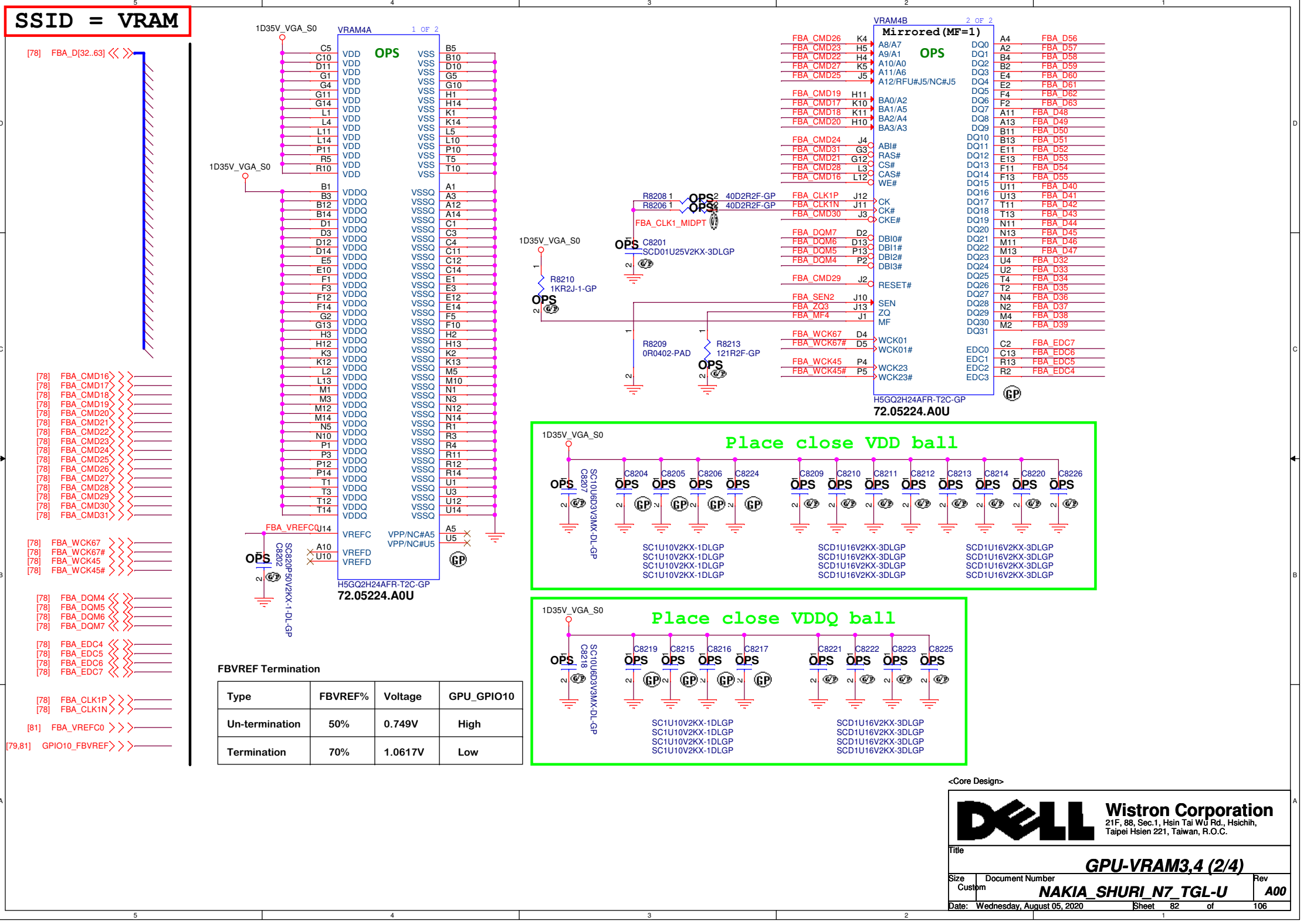
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: A3 | Document Number: NAKIA_SHURI_N7_TGL-U | Rev: A00

Date: Wednesday, August 05, 2020 | Sheet 81 of 106

SSID = VRAM



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM3,4 (2/4)*

Size: Custom | Document Number: *NAKIA_SHURI_N7_TGL-U* | Rev: *A00*

Date: Wednesday, August 05, 2020 | Sheet 82 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 83 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM7,8 (4/4)*

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 84 of 106

Main Func = dGPU_CORE

RT8816B For NVVDD

need 1.8V

Table 1

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

Figure 12. GC6 Voltage Regulator Complex Signal Connection

For tuning VGA_CORE sequence.

N17S-G2
EDP-Continuous : 28.6 A
EDP-Peak : 60.3 A

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A

OCP setting

SS setting

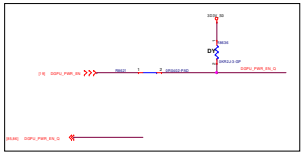
Place Near GPU (NVVDDS)
1X330uF (Poscap) - PT8511 (Page85)

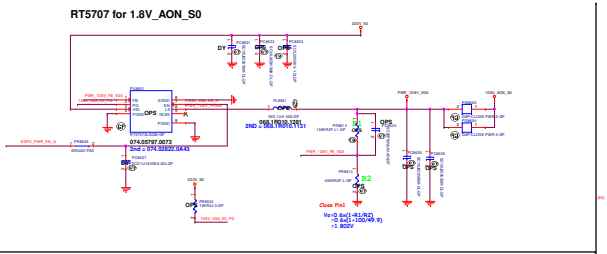
<Core Design>

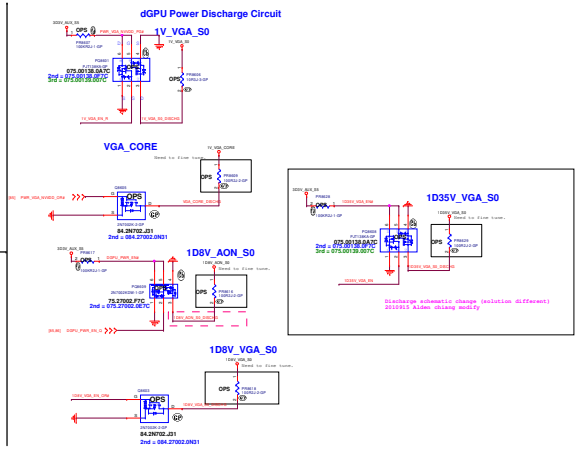
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

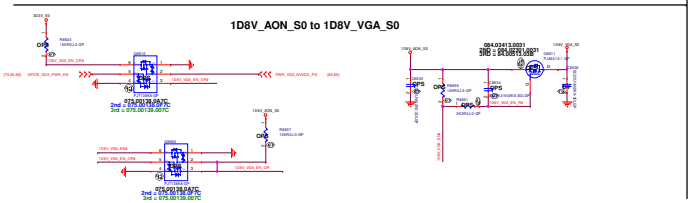
Title: VGA Power B
Size: A1
Document Number: Vader15"/17" CML
Rev: A00
Date: Wednesday, August 05, 2020
Sheet 85 of 106

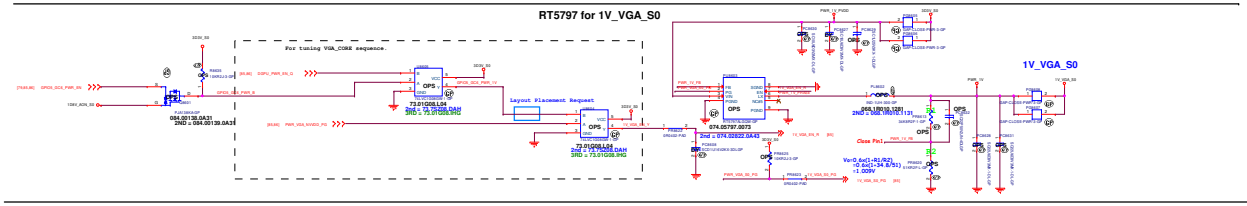
Main Func = dGPU



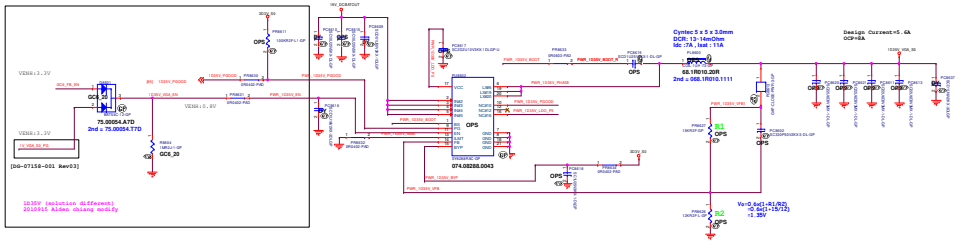








1D35V_VGA_S0



Wistron Corporation
DISCRETE VGA POWER
Vostro15"/17" CMI

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A4	***NAKIA_SHURI_N7_TGL-U***	

Date: Wednesday, August 05, 2020 Sheet 87 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

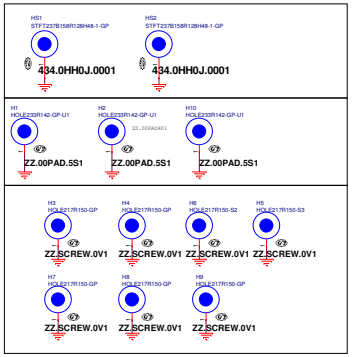
Title

Reserved

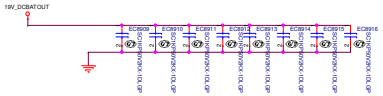
Size	Document Number	Rev
A4	*NAKIA_SHURI_N7_TGL-U*	*A00*

Date: Wednesday, August 05, 2020 Sheet 88 of 106

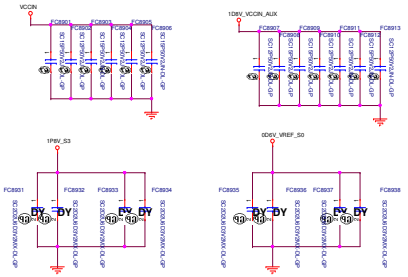
Main Func = UnusedParts



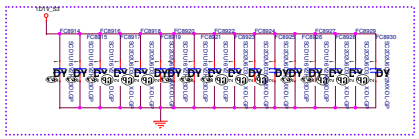
Main Func = EMI Capacitors



Main Func = RF Capacitors



EMC CAPS - PLACE <4mm FROM SOC VDDQ,
WITH EACH PAIR <12mm APART



<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A3	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 04, 2021 Sheet 69 of 156

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	*NAKIA_SHURI_N7_TGL-U*	*A00*

Date: Wednesday, August 05, 2020 Sheet 90 of 106

Main Func = TPM

[15,18,24,25] SPI0_SI_CPU
[18] SPI0_CS_CPU_N2
[18,24,25] SPI0_CLK_CPU
[18,24,25] SPI0_SO_CPU
[17] SIO_SLP_S0#
[17,61,63,71,76] PCH_PLTRST#
[20] TPM_SPI_IRQ#
[17] TPM_SEL

3D3V_S0 R9102 1 2 0R0402-PAD 3D3V_TPM
TPM C9109 SC10U6D3V3MX-DL-GP
TPM C9112 SCD1U16V2KX-3DLGP
TPM C9113 SCD1U16V2KX-3DLGP

3D3V_S5_VCCPRIM R9148 1 TPM 10KR1J-GP SPI_CS2#_IC

3D3V_TPM R9151 1 TPM 2 10KR1J-GP
SPI_IRQ#_TPM2 R9124 1 2 0R0402-PAD TPM_SPI_IRQ#

3D3V_TPM 5mA
TPM C9104 SCD1U16V2KX-3DLGP

3D3V_S5 C9106 SC10U6D3V2MX-2-GP 40mA
TPM C9108 SCD1U16V2KX-3DLGP

SPI0_SI_CPU R9133 1 TPM 2 33R2J-2-GP SPI_SI_ROM_TPM
SPI0_SO_CPU R9132 1 TPM 2 33R2J-2-GP SPI_SO_ROM_TPM
SPI0_CS_CPU_N2 R9130 1 TPM 2 0R0402-PAD-7-NP-GP SPI_CS2#_IC
SPI0_CLK_CPU R9138 1 TPM 2 33R2J-2-GP SPI_CLK_ROM_TPM
PCH_PLTRST#

U9101 TPM
8 VHIO
22 VHIO
1 VSB
21 MOSI/GPIO7
24 MISO
20 SCS#/GPIO5
19 SCLK
17 PLTRST#
16 GND
23 GND
33 GND
2 NC#2
3 NC#3
5 NC#5
29 SDA/GPIO0
30 SCL/GPIO1
18 PIRQ#/GPIO2
6 GPIO3
13 GPIO4
4 PP/GPIO6
7 NC#7
9 NC#9
10 NC#10
11 NC#11
12 NC#12
14 NC#14
15 NC#15
25 NC#25
26 NC#26
27 NC#27
28 NC#28
31 NC#31
32 NC#32
NPCT750JABYX-GP
071.00750.0E03

TPM_GPIO0 R9121 1 DY 2 0R2J-2-GP SIO_SLP_S0#
SPI_IRQ#_TPM2
TPM_GPIO4 R9118 1 DY 2 2K2R2F-GP SPI0_CS_CPU_N2

R9133/R9132/R9130/R9138	
SPI ROM	33 ohm 64.33R05.6DL
G3 Sharing	15 ohm 63.15034.1DL

1D8V_S5 R9134 1
NON-TPM 10KR2J-3-GP
TPM_SEL
R9135 1
TPM 10KR2J-3-GP

ID	Description	Setting	Mapping
TPM_SEL	TPM SUPPORT	1	NON-TPM
		0	TPM

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPM2.0
Size: A4 | Document Number: Shuri 13" CML-U | Rev: A00
Date: Wednesday, August 05, 2020 | Sheet 91 of 106

Main Func = FPR

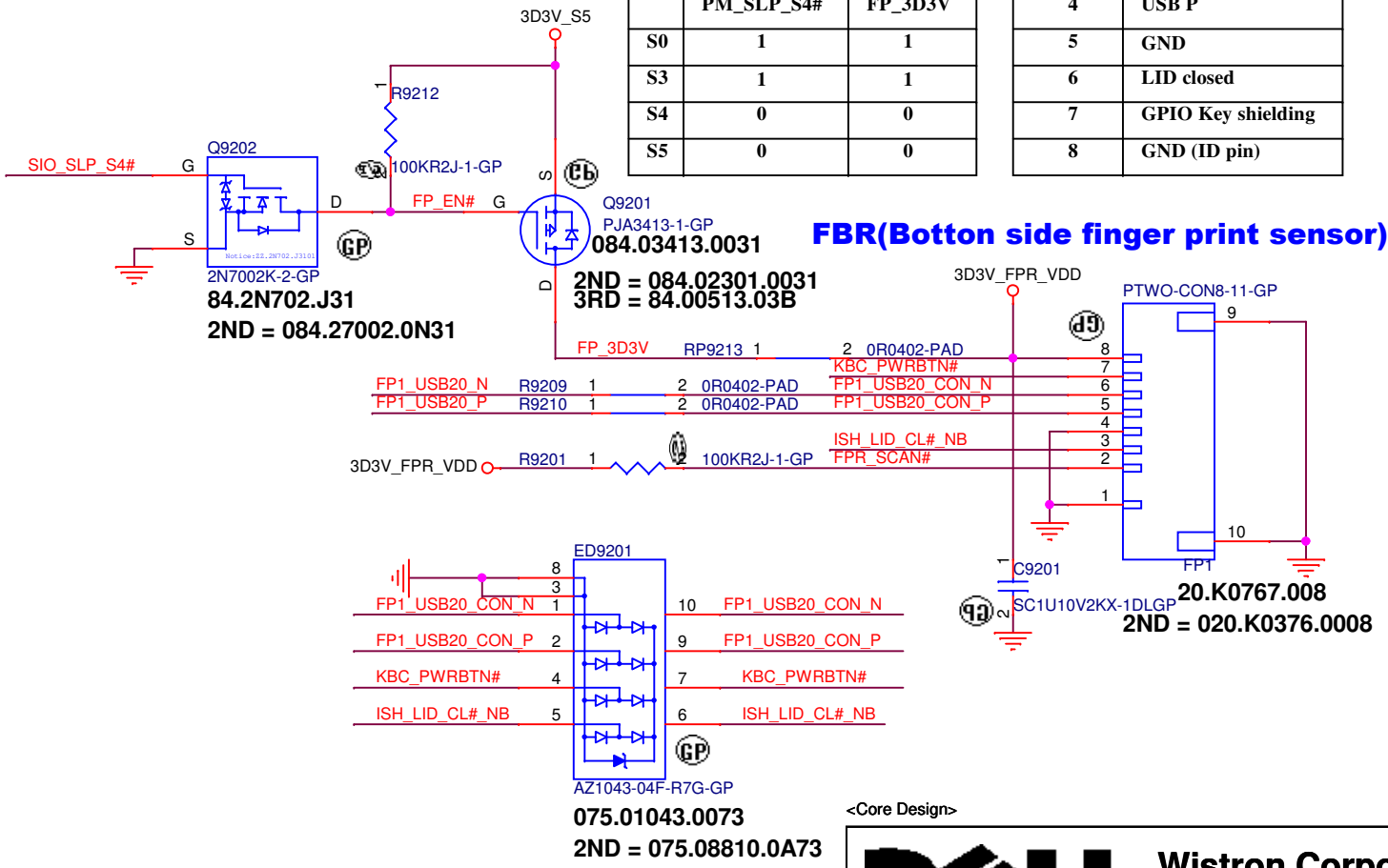
[16] FP1_USB20_N
[16] FP1_USB20_P
[24] FPR_SCAN#
[24,64] KBC_PWRBTN#
[17,40] SIO_SLP_S4#
[20,24,67] ISH_LID_CL#_NB

	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0

GF5288WN1+GF128A+GM168 Module design

CN PIN Map

Pin NO.	INFO
1	VCC 3.3V
2	PWBTN
3	USB N
4	USB P
5	GND
6	LID closed
7	GPIO Key shielding
8	GND (ID pin)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Finger Print*

Size	Document Number	Rev
A4	*NAKIA_SHURI_N7_TGL-U*	*A00*

Date: Wednesday, August 05, 2020 Sheet 92 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	***NAKIA_SHURI_N7_TGL-U***	

Date: Wednesday, August 05, 2020 Sheet 93 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	*NAKIA_SHURI_N7_TGL-U*	*A00*

Date: Wednesday, August 05, 2020 Sheet 94 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A4	*NAKIA_SHURI_N7_TGL-U*	*A00*

Date: Wednesday, August 05, 2020 Sheet 95 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	*NAKIA_SHURI_N7_TGL-U*	*A00*

Date: Wednesday, August 05, 2020 Sheet 96 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 97 of 106

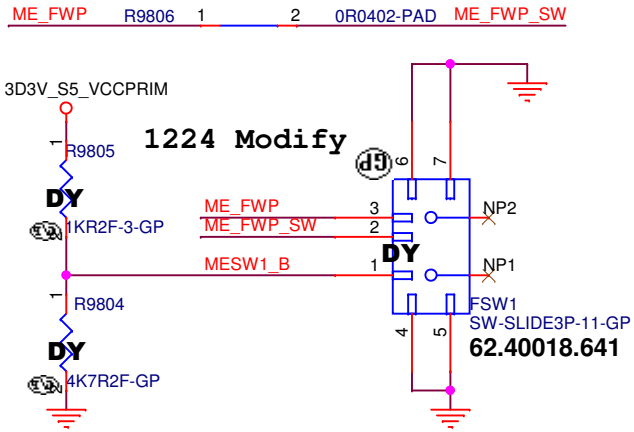
Main Func = SWITCH

[24] ME_FWP >>>

[19] ME_FWP_SW <<<

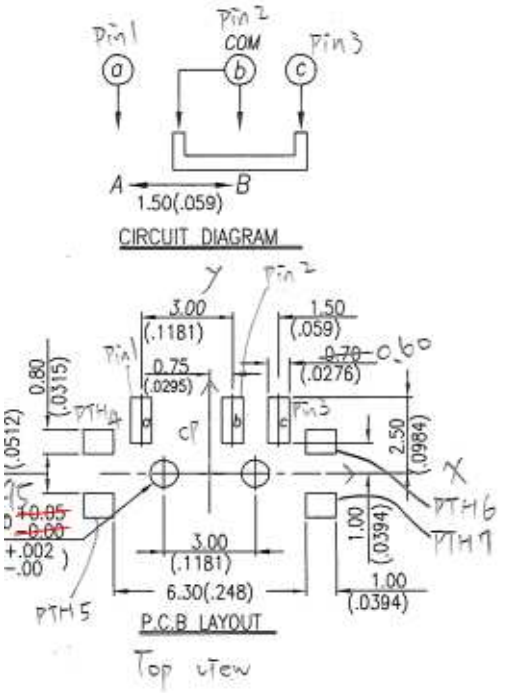
Firmware SW

Default setting:pull LOW
DY for MP



	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

*Symbol same as 62.40018.461.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT_Switch***

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 98 of 106

<Core Design>

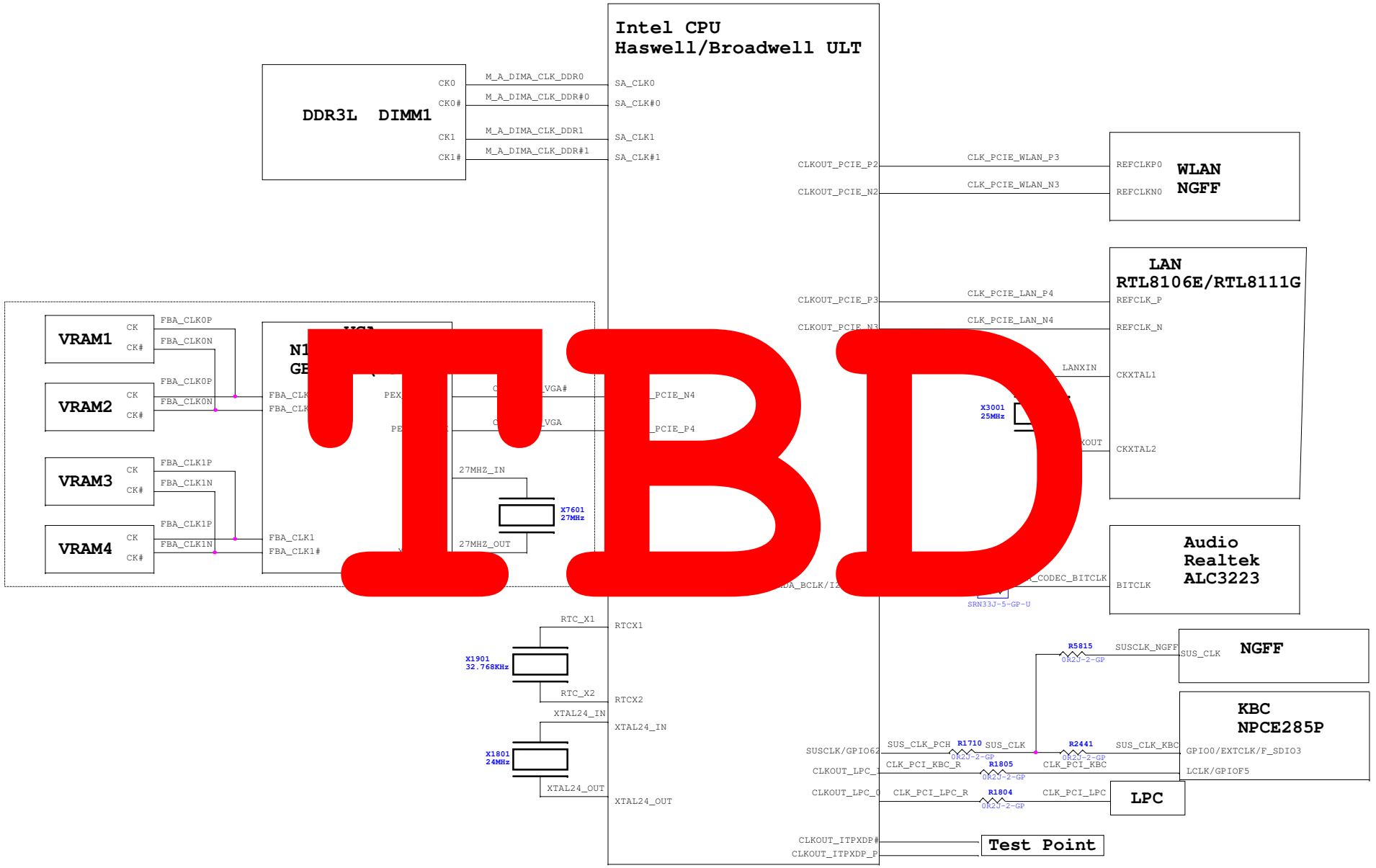
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Debug (XDP/HDT conn)***

Size	Document Number	Rev
A4	***NAKIA_SHURI_N7_TGL-U***	***A00***

Date: Wednesday, August 05, 2020 Sheet 99 of 106

CLK Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CLK Block Diagram	
Size: A2	Document Number: NAKIA_SHURI_N7_TGL-U	Rev: A00
Date: Wednesday, August 05, 2020	Sheet 100 of 106	

Change notes –

DATE	VERSON	DATE	Page	Modify List	OWNER

<Core Design>

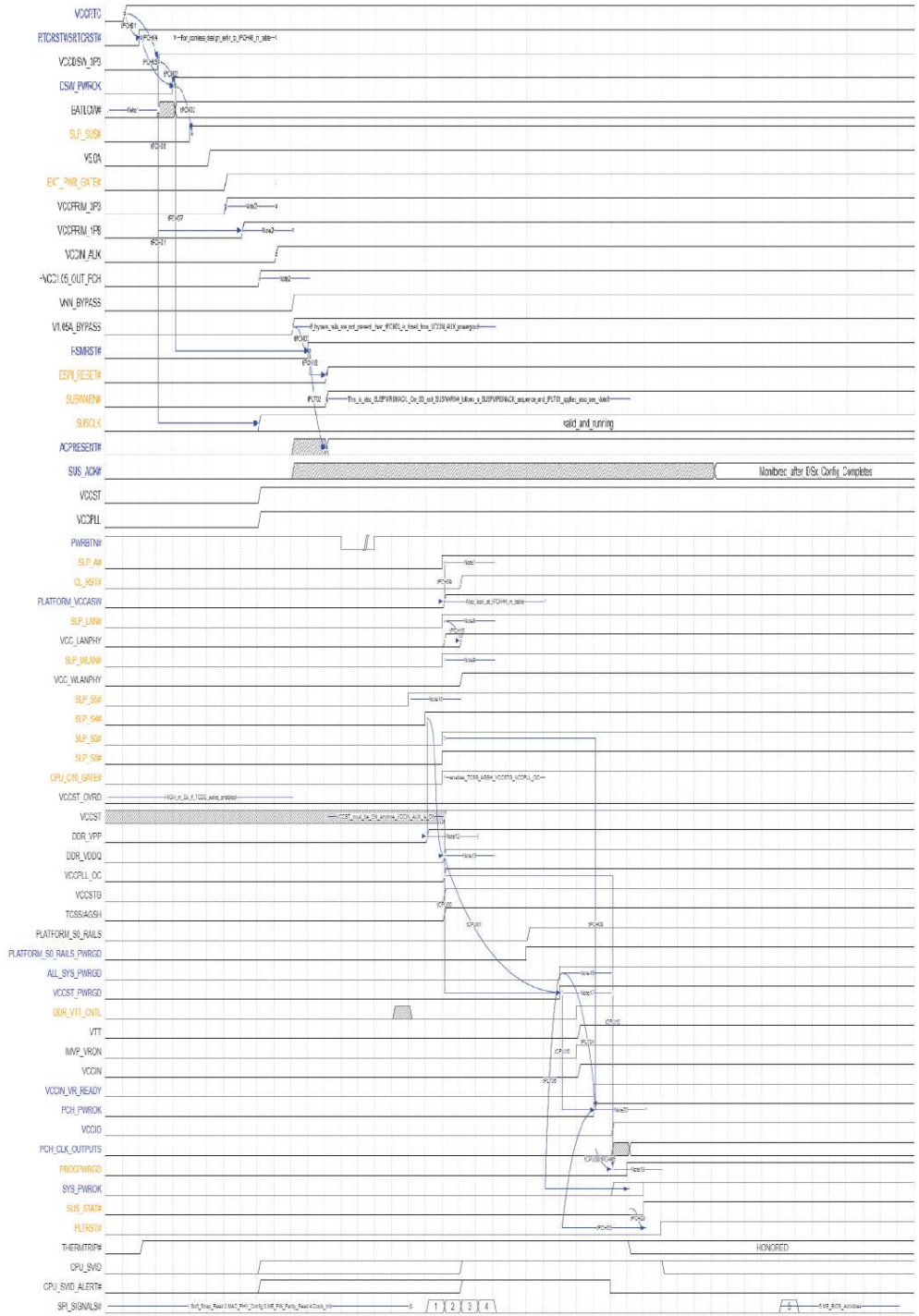
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Change History***

Size	Document Number	Rev
A3	*NAKIA_SHURI_N7_TGL-U*	*A00*

Date: Wednesday, August 05, 2020 Sheet 101 of 106

G3 to S5 Sequence

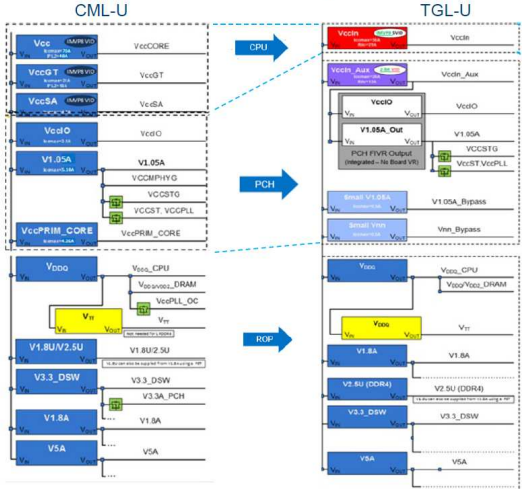


<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **Power Sequence**		
Size: A2	Document Number: NAKIA_SHURI_N7_TGL-U	Rev: A00
Date: Wednesday, August 05, 2020	Sheet 102 of 106	

CML-U and TGL-U Power and VR Considerations (Cont..)

- TGL-U has IMVP9/FIVR implementation for both CPU and PCH power rails, whereas CML-U has IMVP8/discrete VRs for different power rails.
  - TGL-U IMVP9 Power map:
    - VCCIN: VCC_CORE and VCCGT
    - VCCIN_AUX: VCCSA, VCCIO, VNN, V1.05
  - CML-U IMVP8 Power map:
    - VCC_CORE
    - VCCGT
    - VCCSA



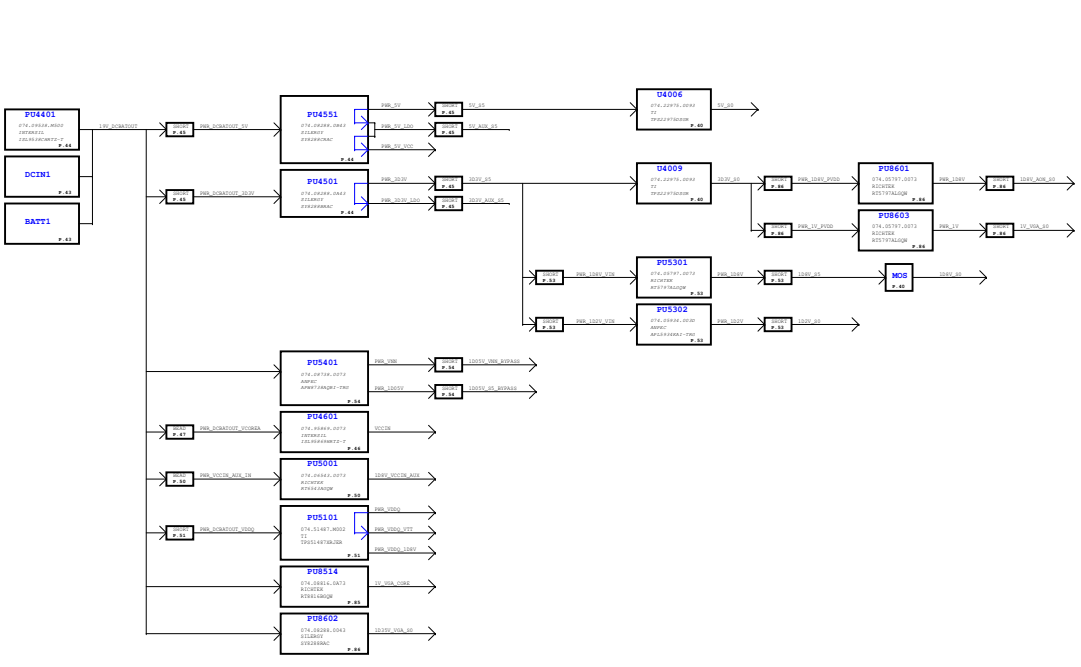
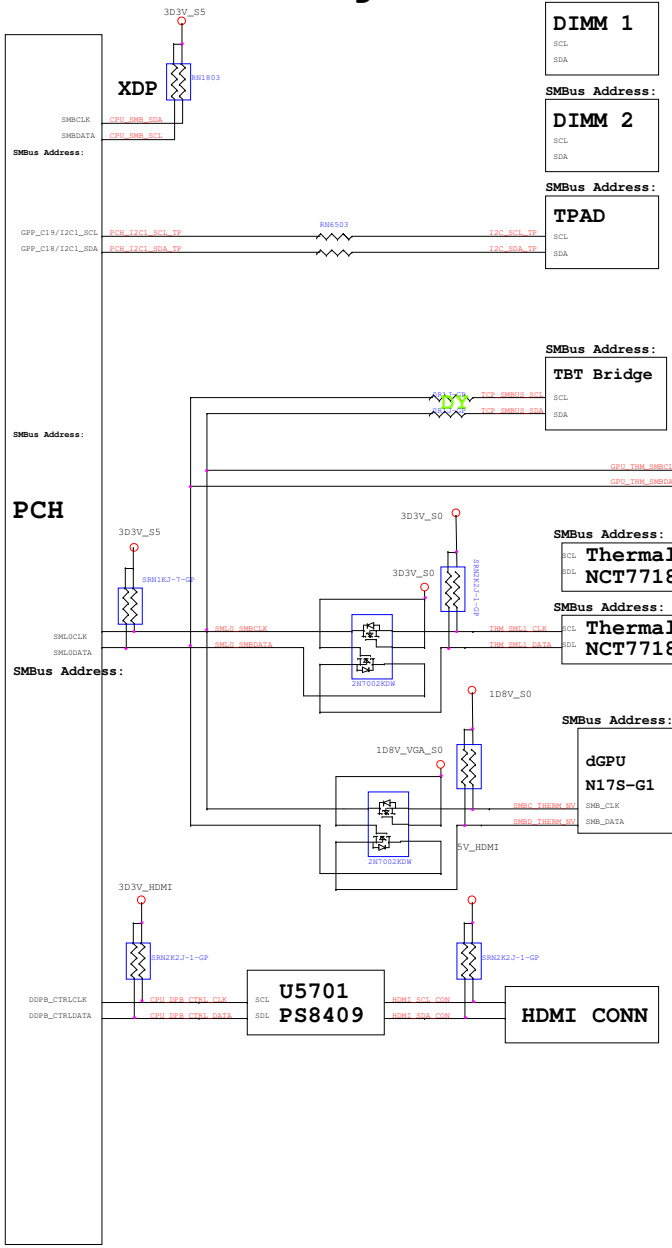


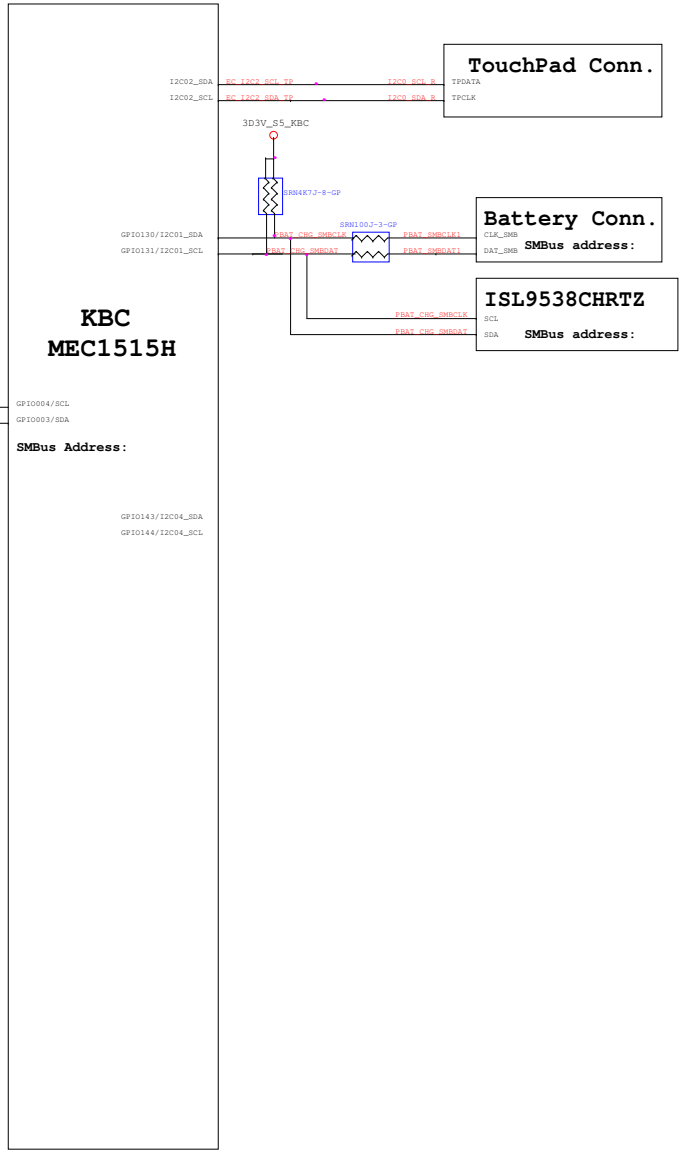
Table 10. Power Rail Descriptions for TGL U

Name	Description
VCCIN_AUX	**FIVR Input rail:** 1.8V
VCC_VNNEXT_1P05	**Used for FIVR PRIM_CORE bypass mode during Sx**: 1.05V
VCC_V1P05EXT_1P05	**Used for FIVR PCH IO bypass mode during Sx:** 1.05V
VCCA_CLKLDO_1P8	**Analog supply for internal clocks:** 1.8V
VCCPRIM1P05 _OUT_PCH	**1.05V Primary Well**: for CNVi and other internal I/O blocks.
VCCDSW_1P05	**Deep Sx Well**: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic.
VCCPRIM_1P8	**1.8V Primary Well**.
VCCPRIM_3P3	**3.3V Primary Well**.
VCCPGPPR	**Audio Power 3.3V, 1.8V, or 1.5V**. If powered at 3.3V, the 3.3V supply can come from VCCPRIM_3P3 supply. If powered at 1.8V, the 1.8V supply can come from VCCPRIM_1P8 supply.
VCCDSW_3P3	**3.3V Deep Sx Well**.
VCCRTC	**RTC Well Supply**. This rail can drop to 2.0V if all other planes are off. This power is not expected to be shut off unless the RTC battery is removed or drained. *Notes:* 1. VCCRTC nominal voltage is 3.0V. This rail is intended to always come up first and always stay on. It should NOT be power cycled regularly on non-coin battery designs. Refer to the Platform Design Guide, RTC Design Guidelines chapter for latest design recommendations. 2. Implementation should not attempt to clear CMOS by using a jumper to pull VCCRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
VCCDPHY_1P24	**1.24V for CNVi logic**. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide (PDG) for implementation details.
VCCLDOSTD_0P85	This rail is generated internally and needs to be routed out to the motherboard for decoupling purpose.
VCC1P05 _OUT_FET	**FIVR output rail:** 1.05V, used for CPU rails VCCST/STG.
VSS	Ground

PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 104_SMBUS/I2C BLOCK DIAGRAM

Size	Document Number	Rev
Custom	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 104 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
A2	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 105 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CLK Block

Size	Document Number	Rev
A4	NAKIA_SHURI_N7_TGL-U	A00

Date: Wednesday, August 05, 2020 Sheet 106 of 106